

T490S/X390 Logic Schematics

Jazz/Sideswipe
VER 1.0
Jun/12/2018

BASE LOGIC 1 : Lightsaber-3 Pass-1 VER 0.25 Jul/10/2017
BASE LOGIC 2 : Finn-1 SIT VER 2.01 Jun/28/2017

- 1.TITLE PAGE

2.BLOCK DIAGRAM

3.CPU (1/16): DDI/TYPER-C

4.CPU (2/16): DDR (1/2)

5.CPU (3/16): DDR (2/2)

6.CPU (4/16): MISC/JTAG

7.CPU (5/16): ESPI/SPI/SMBUS/C-LINK

8.CPU (6/16): LPSS/ISH

9.CPU (7/16): AUDIO/SDXC

10.CPU (8/16): PCIE/USB/SATA

11.CPU (9/16): CSI-2/EMMC/CNVI

12.CPU (10/16): CLOCK SIGNALS

13.CPU (11/16): SYSTEM PM

14.CPU (12/16): CPU POWER (1/2)

15.CPU (13/16): CPU POWER (2/2)

16.CPU (14/16): PCH POWER

17.CPU (15/16): GND

18.CPU (16/16): CFG/RESERVED

19.XDP CONNECTOR

20.RTC BATTERY

21.SPI FLASH

22.BLANK

23.BLANK

24.BLANK

25.BLANK

26.BLANK

27.BLANK

28.BLANK

29.BLANK

30.BLANK

31.BLANK

32.BLANK

33.DDR4 SUB CHANNEL-A

34.DDR4 SUB CHANNEL-B

35.DDR4 SUB CHANNEL-C
- 36.DDR4 SUB CHANNEL-D

37.BLANK

38.BLANK

39.BLANK

40.BLANK

41.BLANK

42.BLANK

43.BLANK

44.BLANK

45.BLANK

46.BLANK

47.BLANK

48.BLANK

49.BLANK

50.BLANK

51.LCD INTERFACE

52.LID/CAMERA/MIC/TOUCH INTERFACE

53.BLANK

54.HDMI CONNECTOR

55.ALPIKE RIDGE (1/2)

56.ALPIKE RIDGE (2/2)

57.BLANK

58..BLANK

59.USB PD CONTROLLER

60.BLANK

61.Type-C Switch

62.DOCKING CONNECTOR

63.THUNDERBOLT CONNECTOR

64.M.2 SOCKET 3 MODULE I/F

65.BLANK

66.M.2 TYPE 2230

67.M.2 SOCKET 2 MODULE I/F

68.DDI DEMUX/HDMI LEVEL SHIFTE

69.USB TYPE-A CONNECTOR

70.USB TYPE-A CONN

- 71.BLANK

72.Smart card reader/FRP/NEC LED

73.GBE JACKSONVILLE

74.BLANK

75.BLANK

76.MEDIA CARD CONTROLLER

77.MEDIA CARD INTERFACE

78.AUDIO ALC3287

79.AUDIO CONNECTOR

80.AUDIO JACK SENSE

81.AUDIO EXT MIC I/F

82.AUDIO SPEAKER

83.AUDIO BEEP

84.AUDIO Debug port

85.MEC1663(1/3)

86.MEC1663(2/3)

87.MEC1663(3/3)

88.KEYBOARD/TRACK POINT

89.TOUCH PAD/NFC

90.FAN CONNECTOR

91.APS G-SENSOR

92.BLANK

93.SMBUS SWITCH

94.THINK ENGINE-3 (1/2)

95..THINK ENGINE-3 (2/2)

96.BLANK

97.BLANK

98.DISCRETE TPM 2.0
- 99.SCREW HOLES

100.DC-IN

101.BATTERY INPUT

102.BATTERY CHARGER(BQ25700A)

103.DC/DC VCC5M (NB690)

104.DC/DC VCC5M_PD (NB693)

105.DC/DC VCC3M (TPS51393)

106.BLANK

107.DC/DC VCC1R8_SUS (BU90104)

108.DC/DC IMVP8 (MP2949AGQKT)

109.DC/DC VCCPCUCORE (MP86901C)

110.DC/DC VCCGFXCORE_I (MP86901)

111.DC/DC VCCSA (MP86901A)

112.DC/DC VCC1R2A(NB687)

113.BLANK

114.DC/DC VCC1R05_SUS(NB693)

115.BLANK

116.LOAD SW VCCST & VCCSTG

117.LOAD SW LAN

118.LOAD SW B

119.LOAD SW WLAN

120.LOAD SW PCH SUS

JAZZ/SIDESWIPE Block Diagram

Project Code: FT491/FX390

2018 Feb ' 20

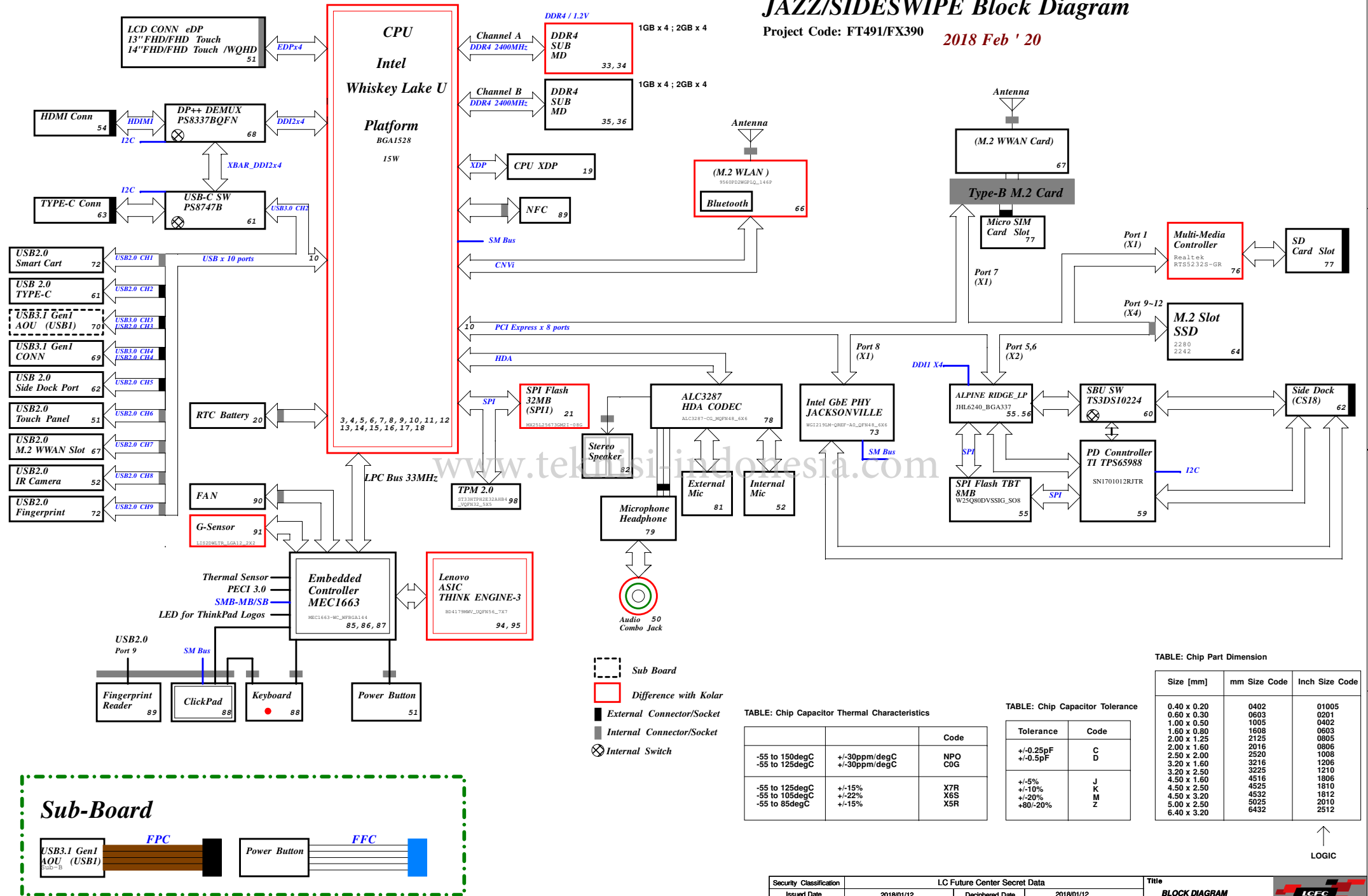


TABLE: Chip Capacitor Thermal Characteristics

Temperature Range	Capacitance Change	Code
-55 to 150degC	+/-30ppm/degC	NPO
-55 to 125degC	+/-30ppm/degC	C0G
-55 to 125degC	+/-15%	X7R
-55 to 105degC	+/-22%	X6S
-55 to 85degC	+/-15%	X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.25pF	C
+/-0.5pF	D
+/-5%	J
+/-10%	K
+/-20%	M
+80/-20%	Z

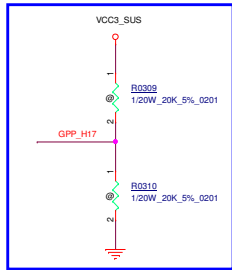
TABLE: Chip Part Dimension


Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20	0402	01005
0.60 x 0.30	0603	0201
1.00 x 0.50	1005	0402
1.60 x 0.80	1608	0603
2.00 x 1.25	2125	0805
2.00 x 1.60	2016	0806
2.50 x 2.00	2520	1008
3.20 x 1.60	3216	1206
3.20 x 2.50	3225	1210
4.50 x 1.60	4516	1806
4.50 x 2.50	4525	1812
4.50 x 3.20	4532	1812
5.00 x 2.50	5025	2010
6.40 x 3.20	6432	2512

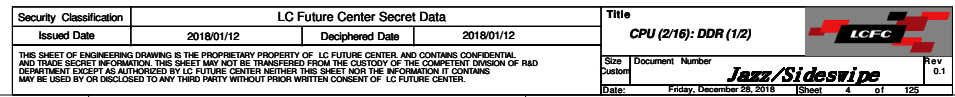
LOGIC

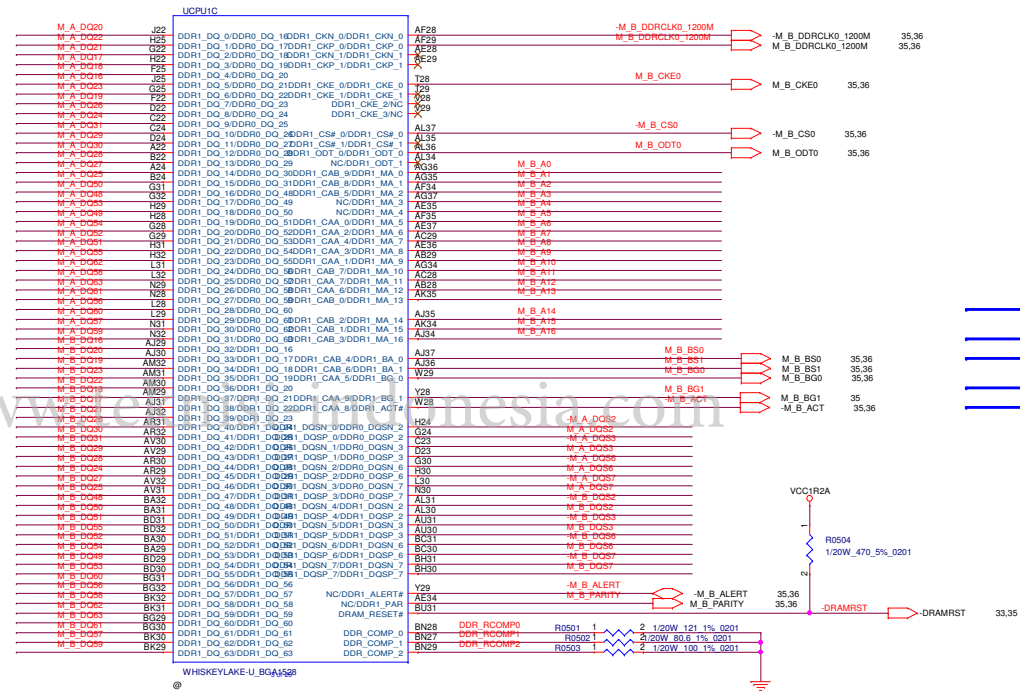
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GPP_E19/DDP1_CTRLDATA/TBT_LXS0_RXD (DDP1 I2C / TBT LXS #0 PINS VCCIO CONFIGURATION)	
GPP_E21/DDP2_CTRLDATA/TBT_LXS1_RXD (DDP2 I2C / TBT LXS #1 PINS VCCIO CONFIGURATION)	
GPP_D10/DDP3_CTRLDATA/TBT_LXS2_RXD (DDP3 I2C / TBT LXS #2 PINS VCCIO CONFIGURATION)	
GPP_D12/DDP4_CTRLDATA/TBT_LXS3_RXD (DDP4 I2C / TBT LXS #3 PINS VCCIO CONFIGURATION)	
HIGH	3.3V
LOW	1.8V



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CPU SKU	U43e	U42
Pin A14	OPCE_RCOMP	Reserved
Pin B14	OPC_RCOMP	Reserved

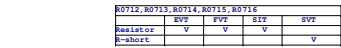
ITP_PMODE (DFX Test Mode)	
HIGH	DFX Test Mode Disabled (Default)
LOW	DFX Test Mode Enabled

GPP_E6 (JTAG ODT Disable)	
HIGH	Enabled
LOW	Disabled

GPP_H2/CNV_BT_I2S_SDO (eSPI Flash Sharing Mode)	
HIGH	Slave Attached Flash Sharing (SAFS) Enabled
LOW	Master Attached Flash Sharing (MAFS) Enabled (Default)



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									Date: <u>File: December 26, 2018</u>		Sheet: 1		124	



DCI Use

PCHHOT R07171 DCI@ 2.020W 4.7K 5% 0201 VCC3_SUS

GPP_B23 / SMLIAUTRT# / PCHHOT#	Intel® DCI- OOB	Rising edge of RSMRST#	<p>This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. <p>This signal is in the primary well.</p>
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Security Classification	LC Future Center Secret Data			Title	CPU (5/16): ESP/SP/SMBUS/C LINK LCFC		
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				Sheet	Jazz/Sideswipe		0.1

TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

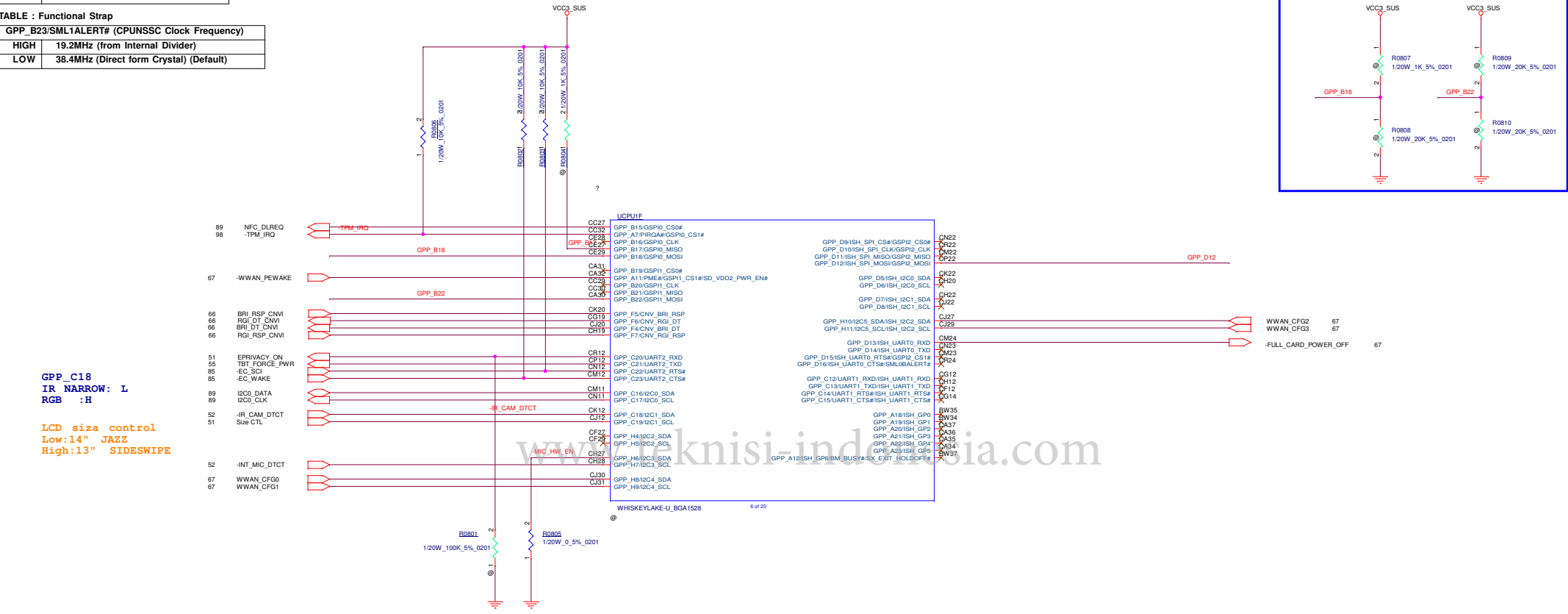
← LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

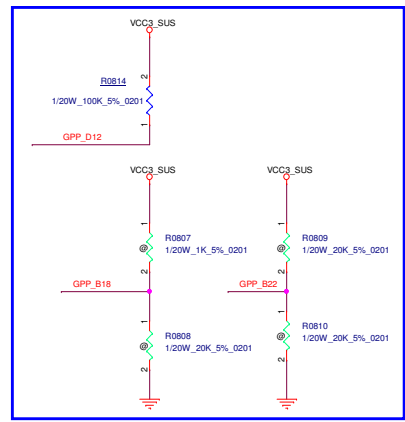
TABLE : Functional Strap

GPP_B23/SML1ALERT# (CPUNSSC Clock Frequency)	
HIGH	19.2MHz (from Internal Divider)
LOW	38.4MHz (Direct form Crystal) (Default)



GPP_C18
IR NARROW: L
RGB :H

LCD siza control
Low:14" JAZZ
High:13" SIDESWIPE

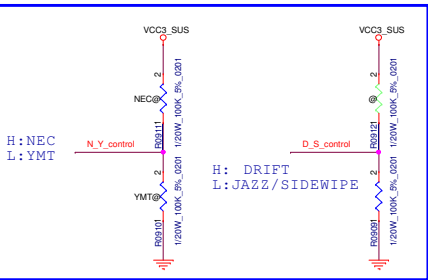
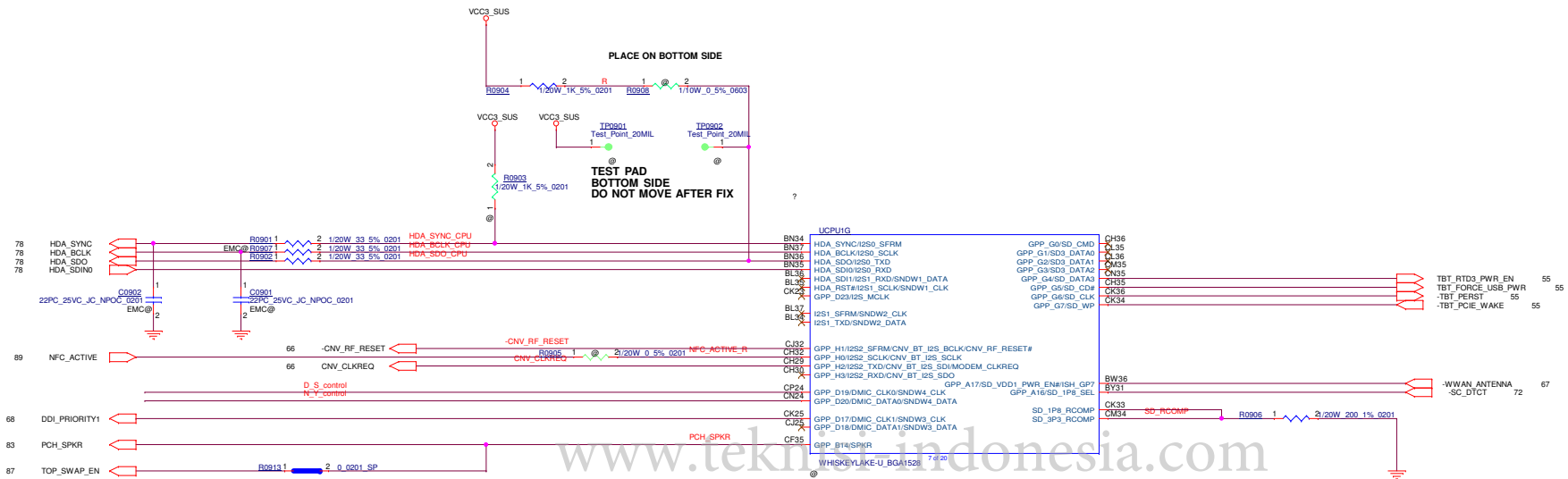


GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWR0K	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. Notes: 1. The internal pull-down is disabled after PCH_PWR0K is high. 2. This signal is in the primary well.
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GPP_B23 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWR0K	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6 0 1 Boot BIOS Destination SPI (Default) LPC Notes: 1. The internal pull-down is disabled after PCH_PWR0K is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GBE LAN. 4. This signal is in the primary well.
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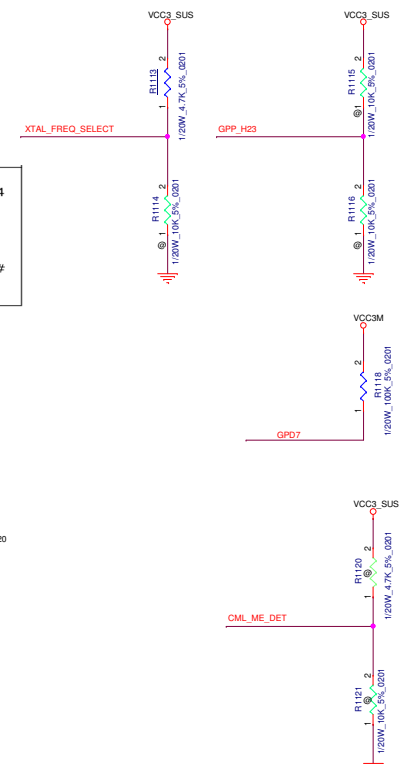
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HDA_SDO/12S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



R0913				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

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					12/28/2018		126	



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				Edition: November 2017			

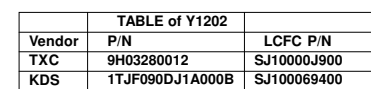
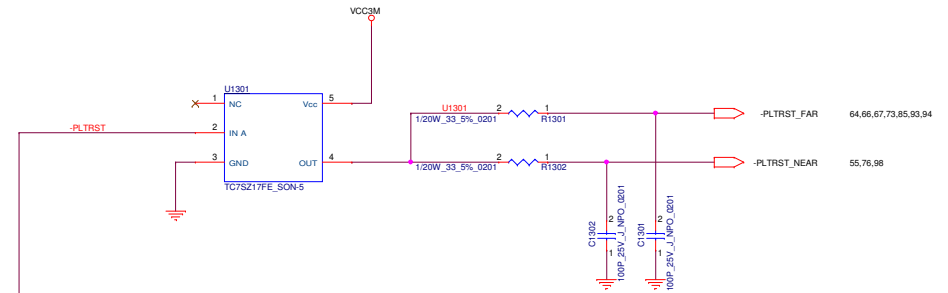
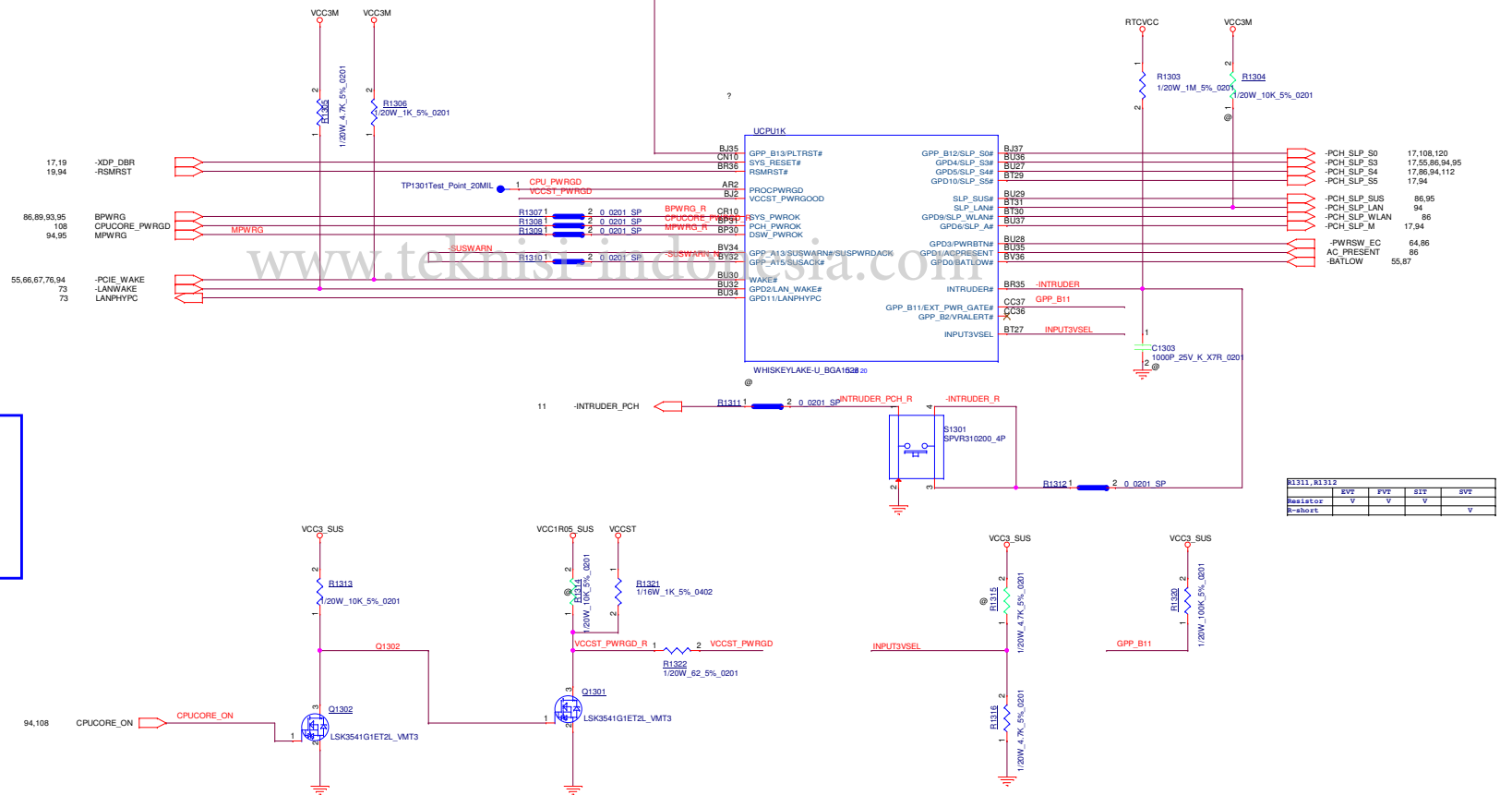


TABLE of U1301		
Vendor	P/N	LCFC P/N
ON	NL17SZ17XV5T2G	SA00005OU00
TI	SN74LVC1G17DRLR	SA00005MG00



R1307, R1308, R1309, R1310				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V



R1311,R1312				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

Check list Suggest

TABLE : Functional Strap

INPUT3VSEL (VCCDSW_3P3)	
HIGH	3.0V
LOW	3.3V

TABLE : Functional Strap

INTRUDER# (SPI Voltage Configuration)	
HIGH	SPI Voltage is 1.8V (Default)
LOW	SPI Voltage is 3.3V

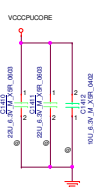
TABLE : Functional Strap

GPD7 (X TAL Input Mode)	
HIGH	X TAL Input is Single Ended
LOW	X TAL is Attached (Default)

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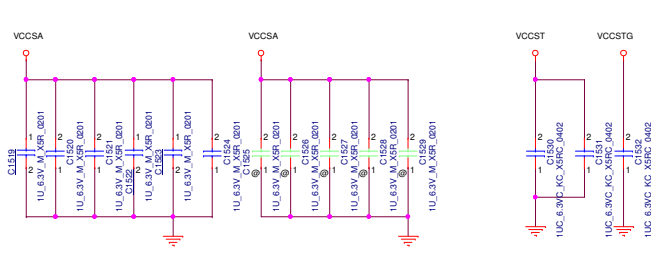
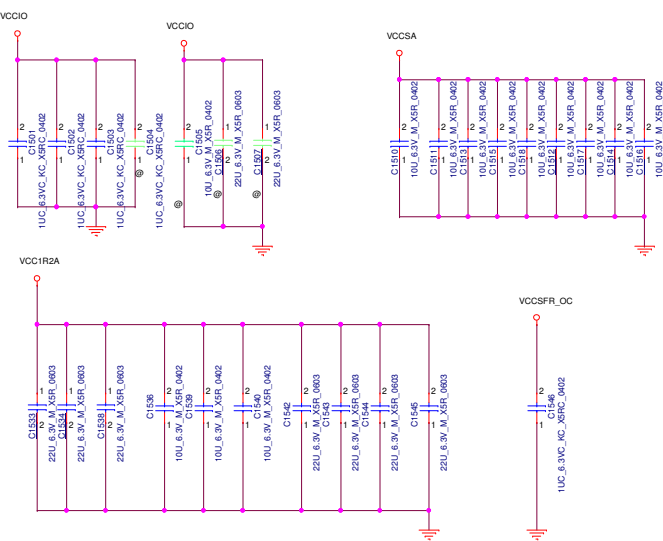
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Title CPU (11/16): SYSTEM PM			
Size Custom	Document Number C	Rev 0.1	
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Date: Friday, December 28, 2018	Sheet 13	of 125	



VccCORE	PDG	PDG
47uF_0805	18	HW:0/PWR:0
22uF_0603	9	HW:0/PWR:24
10uF_0402	22	HW:0/PWR:10
1uF_0402/0201	42	HW:0/PWR:10





VccSA	PDG	LCFC
47uF_0805	2	HW:0/PWR:0
22uF_0805	0	HW:2/PWR:8
10uF_0402	13	HW:5/PWR:7
1uF_0402	0	HW:6/PWR:7

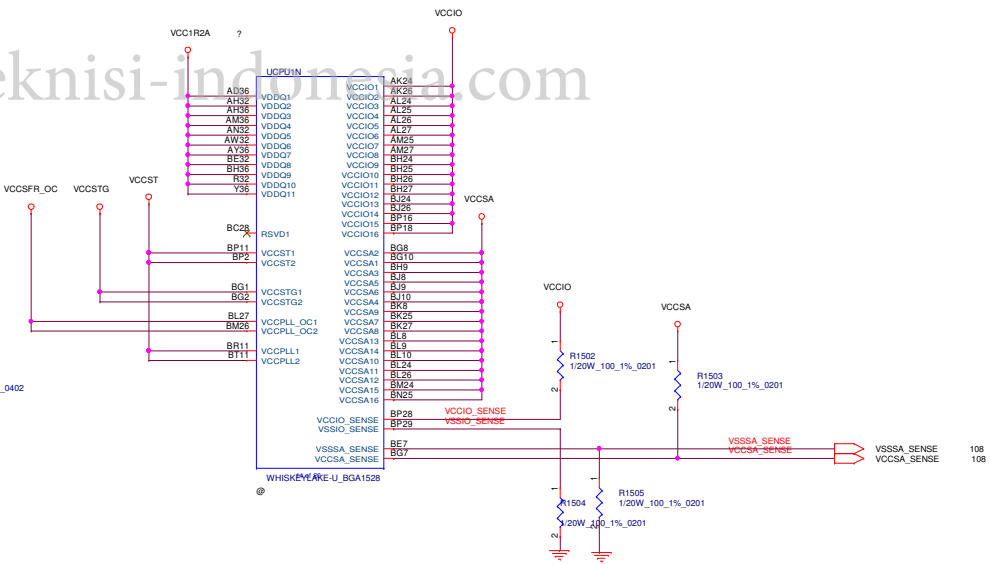
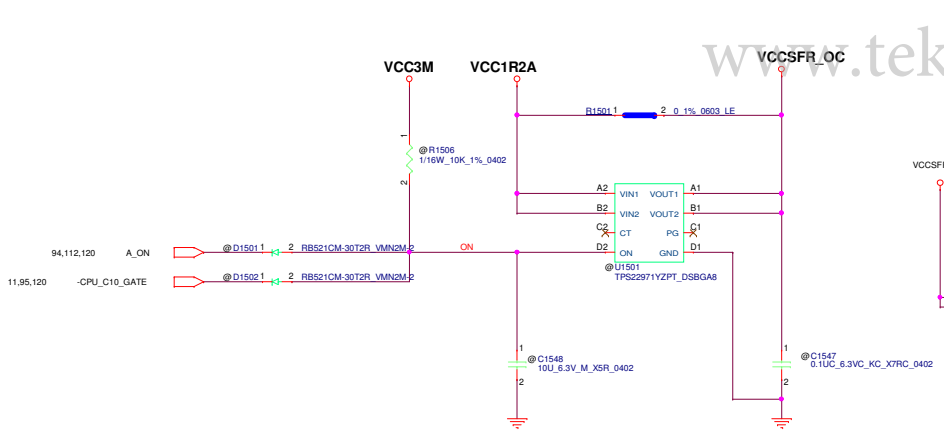
VDDQ	PDG	LCFC
47uF_0805	0	HW:0/PWR:0
22uF_0805	1	HW:7/PWR:6
10uF_0402	9	HW:4/PWR:0
1uF_0402	4	HW:6/PWR:0

VccIO	PDG	LCFC
47uF_0805	0	HW:0/PWR:0
22uF_0805	0	HW:0/PWR:4
10uF_0402	6	HW:0/PWR:0
1uF_0402	4	HW:3/PWR:0

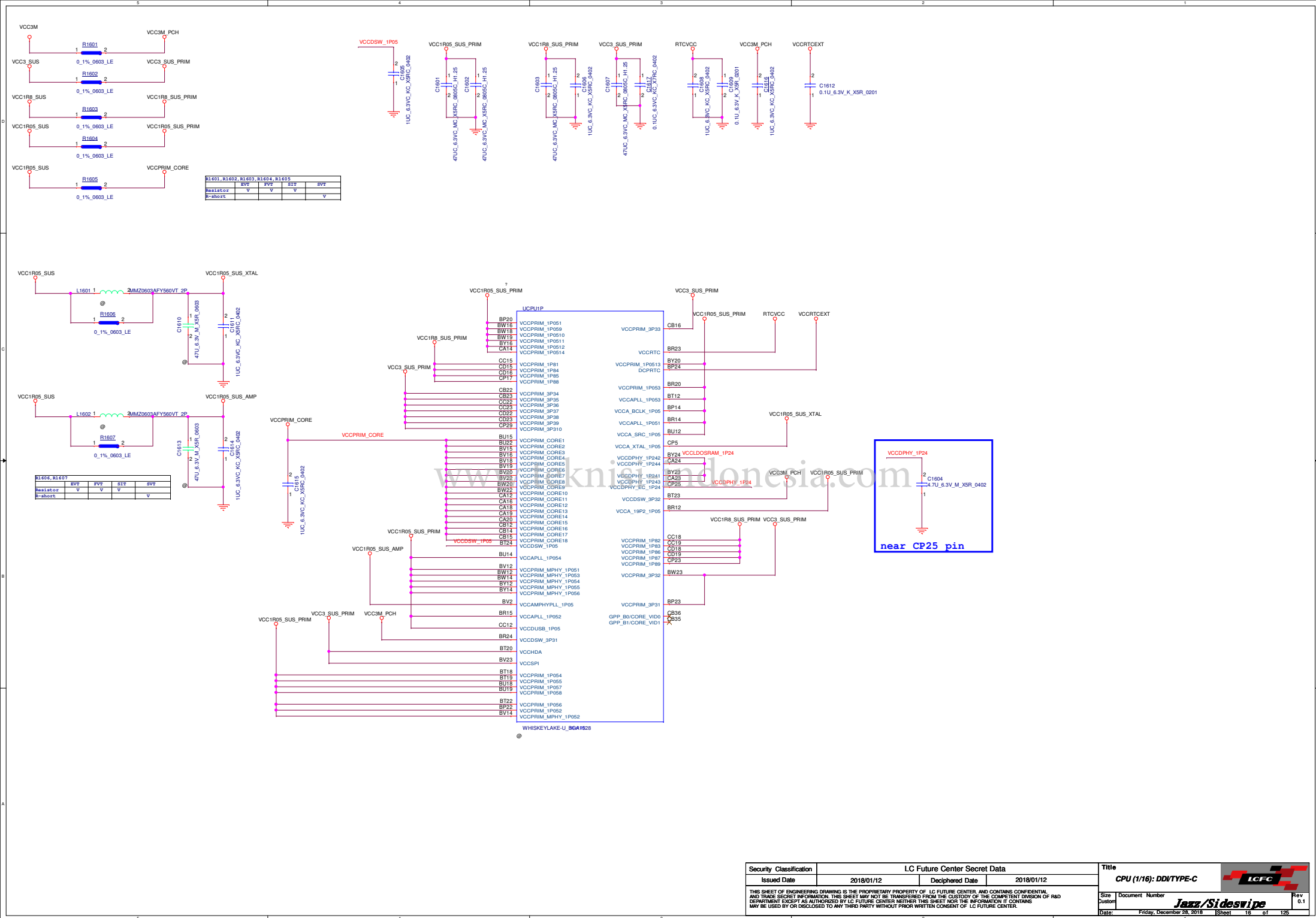
VccPLL	PDG	LCFC
1uF_0402	1	HW:2/PWR:0
0.1uF_0201	1	HW:0/PWR:0

VccPLL_OC	PDG	LCFC
1uF_0402	1	HW:1/PWR:0

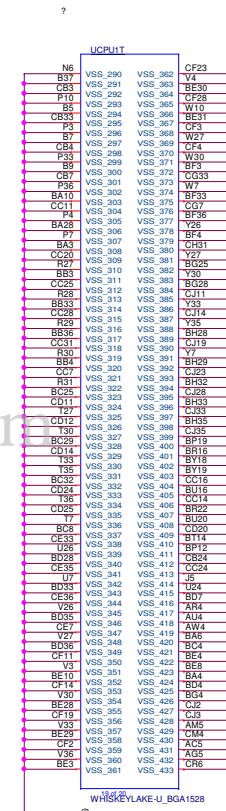
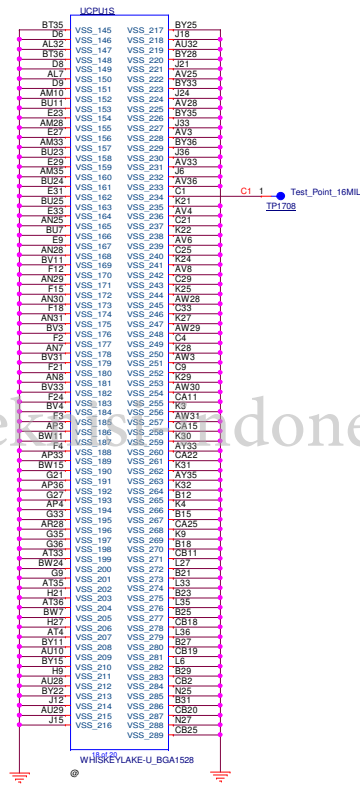
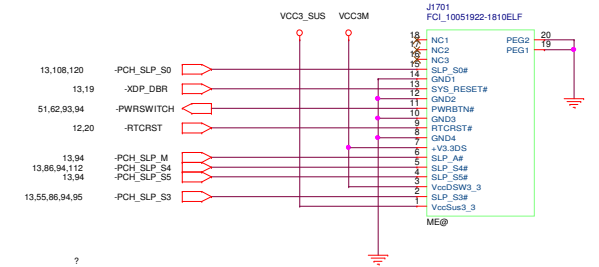
R1501	BVP	FVP	STP	SVT
Resistor	V	V	V	V
Package				





VSSA SENSE	108
VCCSA SENSE	108

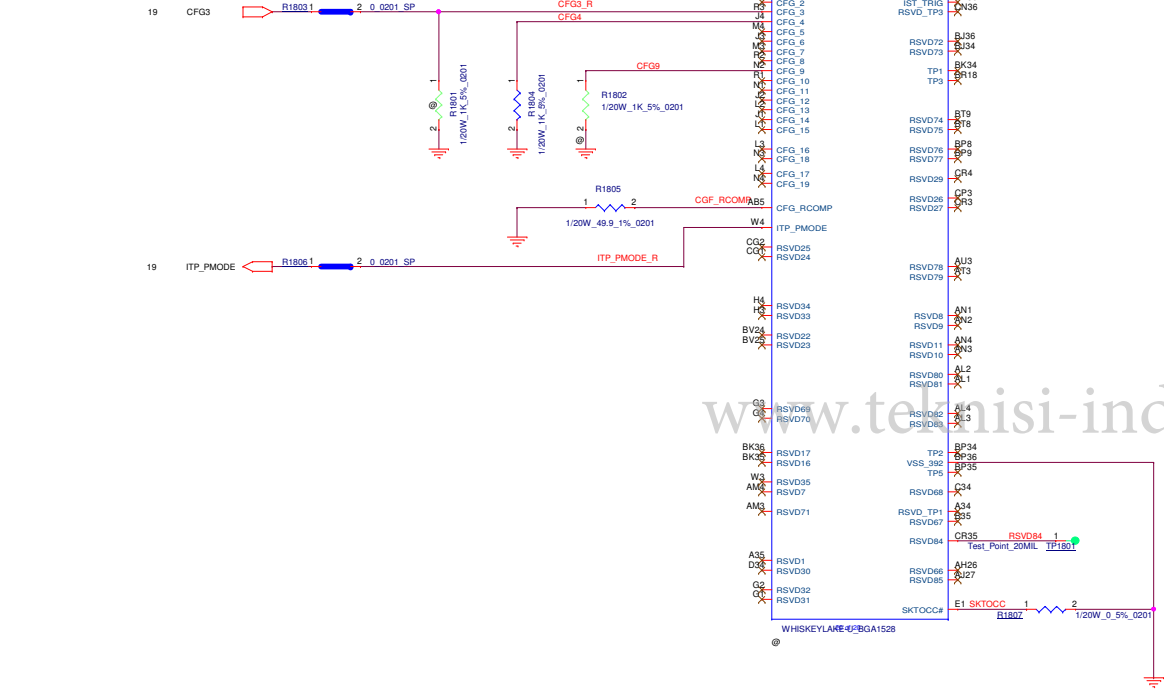


Pinout diagram for the J701 FCI_10051922-1810ELF connector. The diagram shows a 20-pin connector with pins numbered 1 to 20. Pins 1 through 18 are connected to various signals: NC1, NC2, NC3, SLP_S0#, GN1, GN2, PWRBNTN#, GN3, RTCSRST#, GN4, +V3.3DS, SLP_A#, SLP_S4#, SLP_S5#, VcSDSW3_3, VcSSw3_3, and ME#. Pins 19 and 20 are connected to VCC3M and VCC3S respectively. The diagram also shows a ground connection for pin 19.



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				Date:	Friday, December 28, 2018			17 of 125

R1803, R1806	SYM	SYM	SYM	SYM
Resistor	V	V	V	V
W-short				



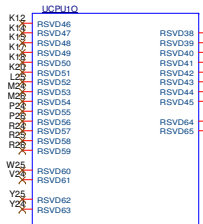
Processor Detect / Socket Occupied: Pulled down directly (0 Ohms) on the processor package to the ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.

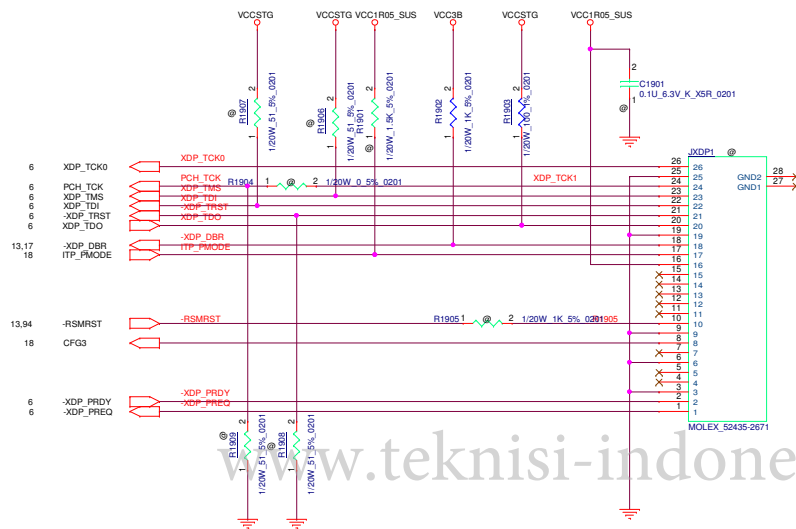
PROC_DETECT#
/SKTOCC#

6.2 Reset and Miscellaneous Signals

Table 6-5. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> 1 = (Default) Normal Operation; No stall. 0 = Stall. CFG[1]: Reserved configuration lane. CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. CFG[3]: Reserved configuration lane. CFG[4]: eDP enable: <ul style="list-style-type: none"> 1 = Disabled. 0 = Enabled. CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* CFG[7]: PEG Training: <ul style="list-style-type: none"> 1 = (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training. CFG[19:8]: Reserved configuration lanes. 	I	GTL	SE	U - Processor Lines. CFG[2], CFG[6:5] and CFG[7] are not relevant for U - Processor Lines.



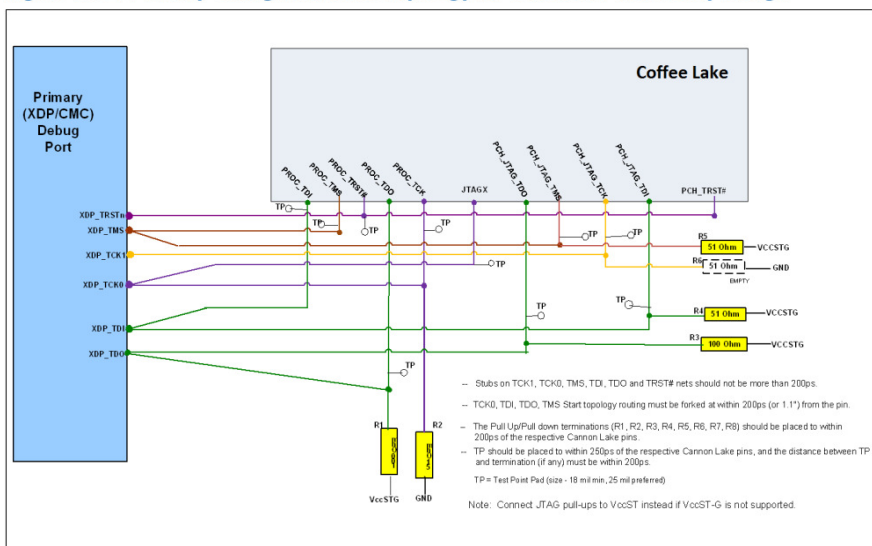


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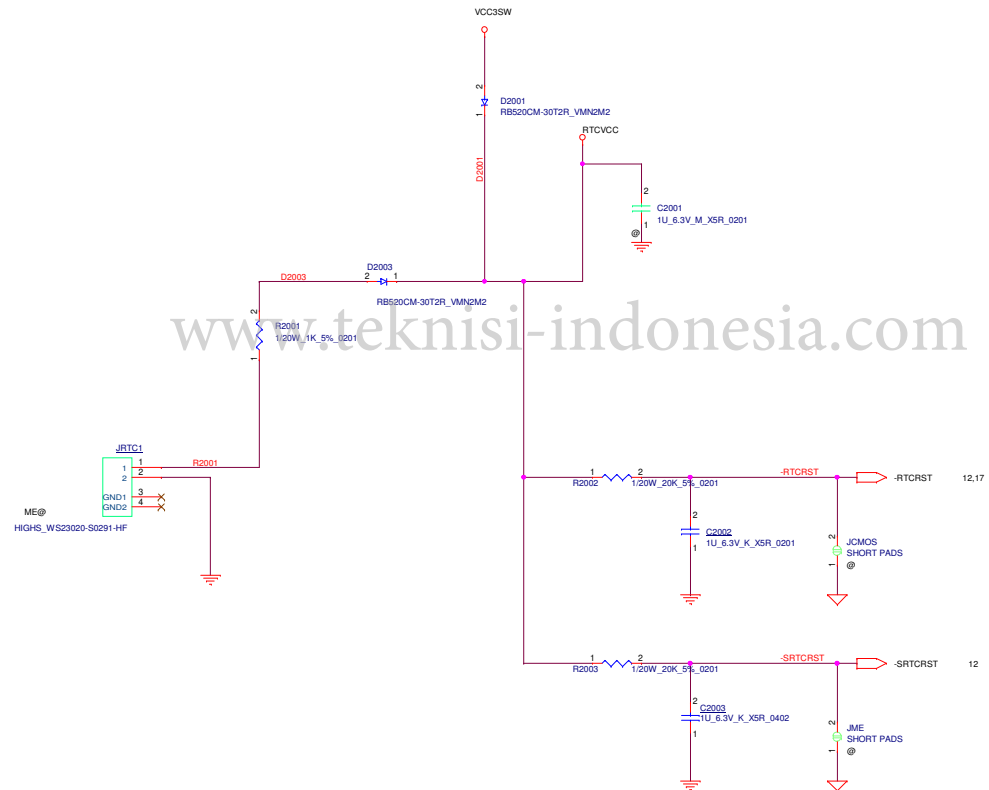
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Page 6	R0610	ASM	NO_ASM
Page 18	R1801	ASM	NO_ASM
Page 19	JXDP1	ASM	NO_ASM
	C1901	ASM	NO_ASM
	R1903	ASM	ASM
	R1902	ASM	ASM
	R1901	ASM	NO_ASM
	R1905	ASM	NO_ASM
	R1904	ASM	NO_ASM


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LOGIC

Figure 13-1. Primary Debug Port-JTAG Topology for Dual Scan Chain Only Design



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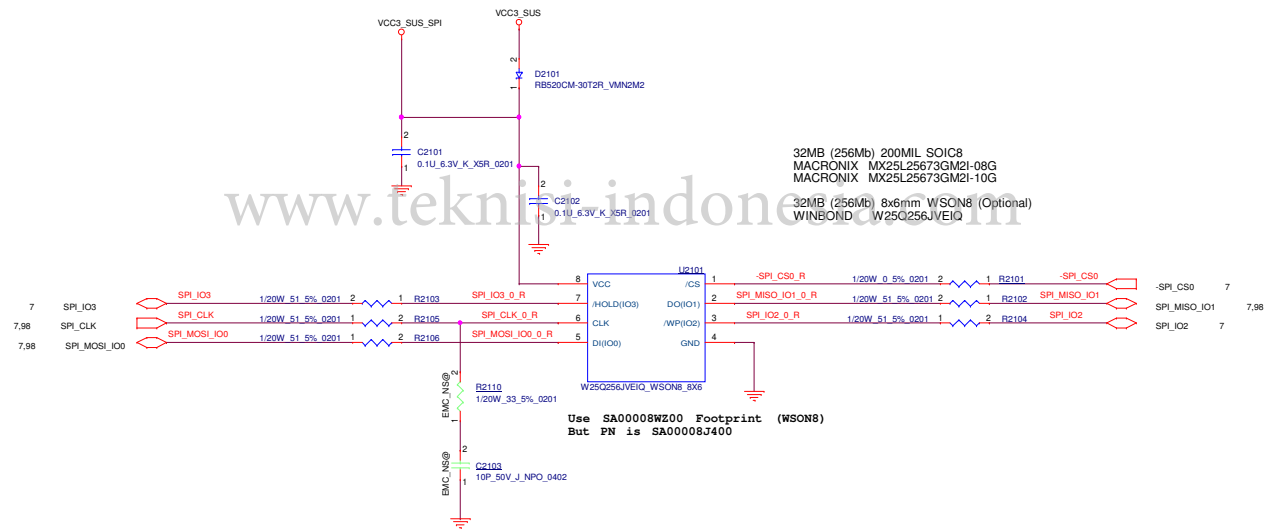



TABLE of TPM (U2101)

Vendor	P/N	LCFC P/N
MXIC	FL 256M MX25L25673GM2I-08G	SA00008J400
WINBOND	FL 256M W25Q256JVEIQ WSON	SA00008WZ00
GigaDevice	256M GD25B256DYIGR WSON	SA00009R800

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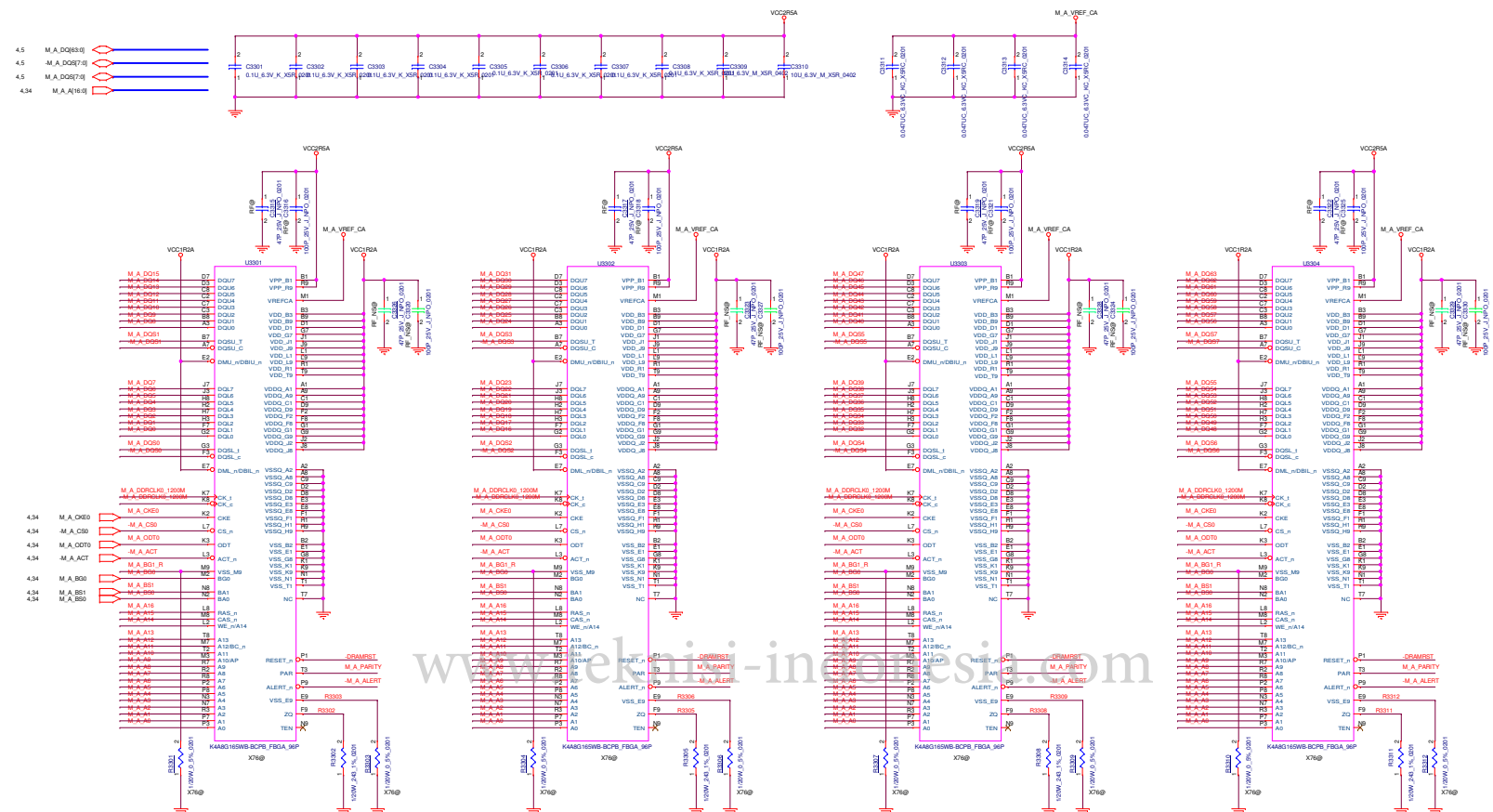


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R3304	ASM	NA
R3307	ASM	NA
R3310	ASM	NA
R3313	NA	ASM
R3316	NA	ASM
R3319	NA	ASM
R3322	NA	ASM

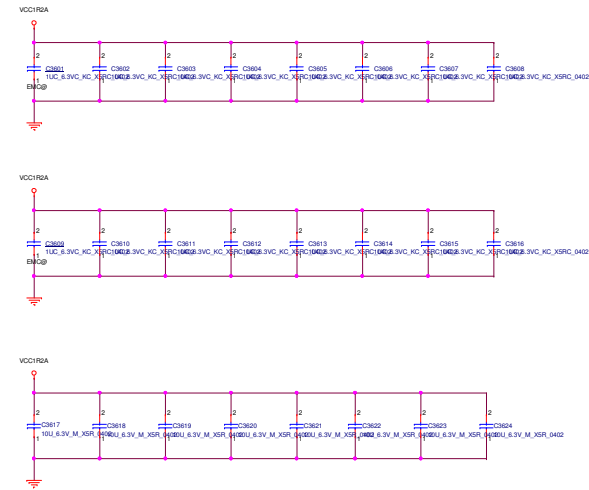
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Micron	8Gbit	MT40A512M16L-075-E	SA00008F920
Micron	16Gbit	MT40A1G16KNR-075-E	SA000090M00
Samsung	8Gbit	K4A8G165WC-BCTD	SA00008PE10
Samsung	16Gbit	K4A8G165WB-MCTD	SA00008WC10
SK hynix	8Gbit	HSAN8G6NCJR-VKC	SA000090T00
SK hynix	16Gbit	HSAN8G6NAMR-UHC	SA00008AD10

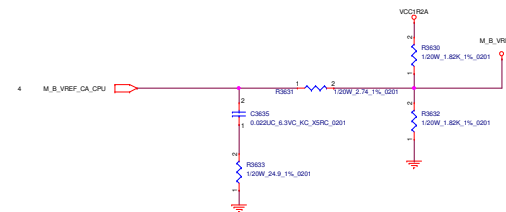
Supplier	Capacity	Supplier's P/N	Package Size	Die	Configuration	VSS_E9	BG1 / VSS	Single Ch	Dual Ch
Micron	8Gbit	MT40A512M16L-075-E	7.5 x 13.5 mm	SDP	8Gb (512Mx16)	0.5%	VSS	4GB	8GB
Micron	16Gbit	MT40A1G16KNR-075-E	7.5 x 13.5 mm	DDP	16Gb (1Gx16)	0.5%	BG1	8GB	16GB
Samsung	8Gbit	K4A8G165WC-BCTD	7.5 x 13.3 mm	SDP	8Gb (512Mx16)	0.5%	VSS	4GB	8GB
Samsung	16Gbit	K4A8G165WB-MCTD	7.5 x 13.3 mm	DDP	16Gb (1Gx16)	0.5%	BG1	8GB	16GB
SK hynix	8Gbit	HSAN8G6NCJR-VKC	7.5 x 13.0 mm	SDP	8Gb (512Mx16)	0.5%	VSS	4GB	8GB
SK hynix	16Gbit	HSAN8G6NAMR-UHC	7.5 x 13.0 mm	DDP	16Gb (1Gx16)	0.5%	BG1	8GB	16GB




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					Date: Friday, December 28, 2018		Sheet 49 of 129

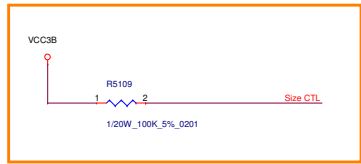
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Date: Friday, December 28, 2018				Sheet 49 of 129		0.1

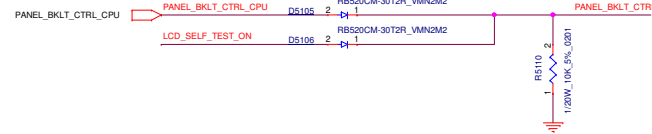
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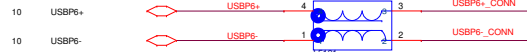
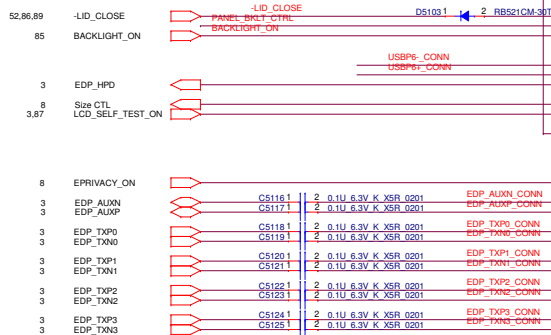
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				Date: Friday, December 28, 2018 (Sheet 50 of 125)	
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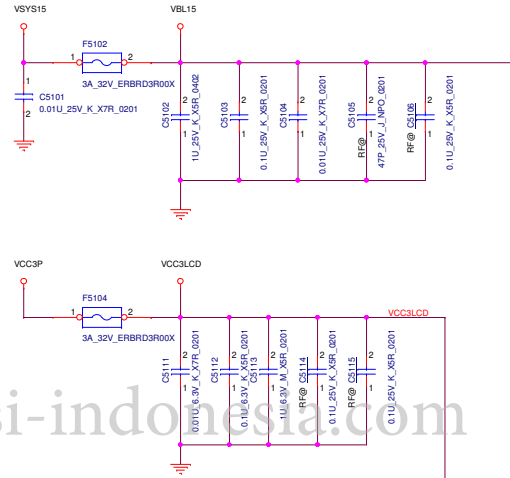
LCD size control
Low: 14" JAZZ
High: 13" SIDESWIPE



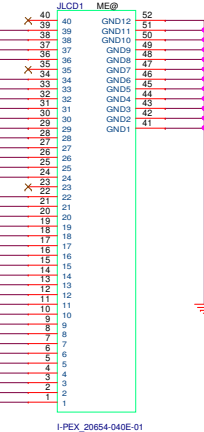
R5107, R5108	RVE	PVE	S1V	SVE
Resistor	V			
R-short				



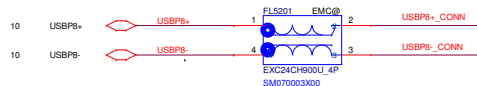
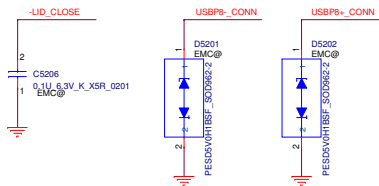
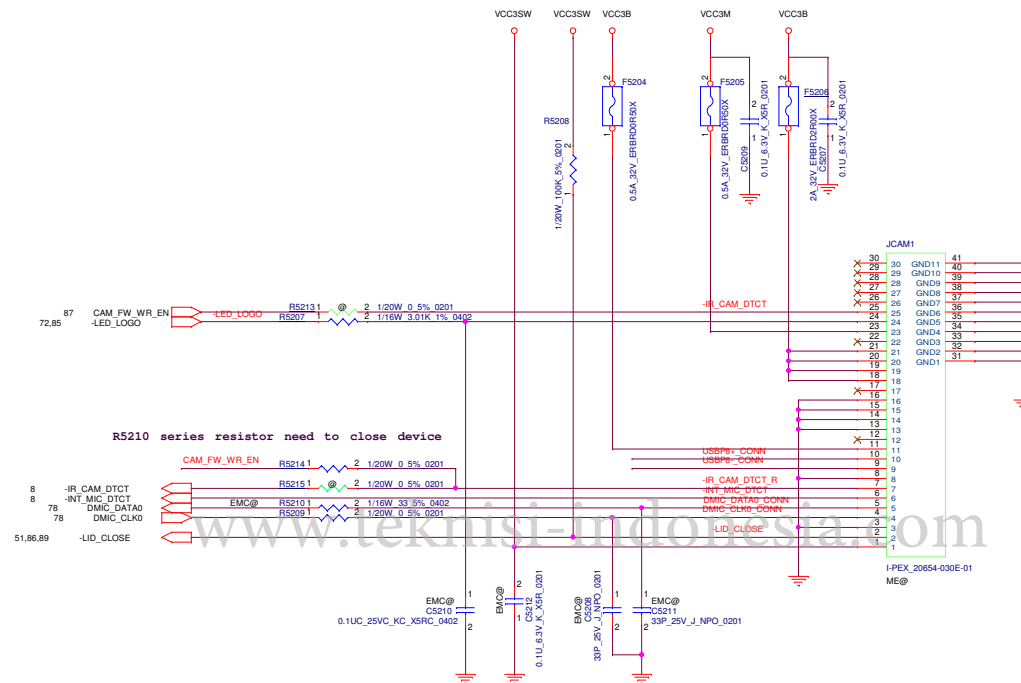
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LCD CONNECTOR



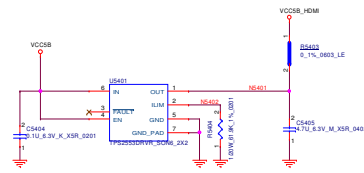
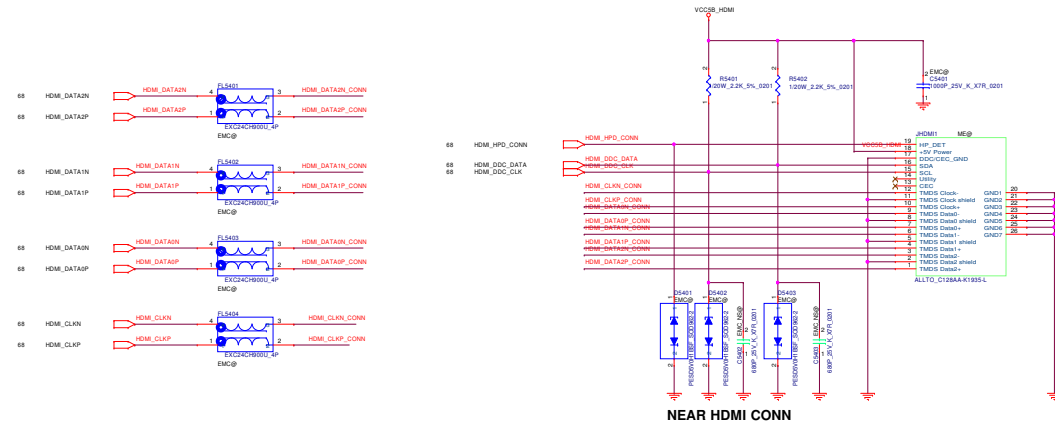
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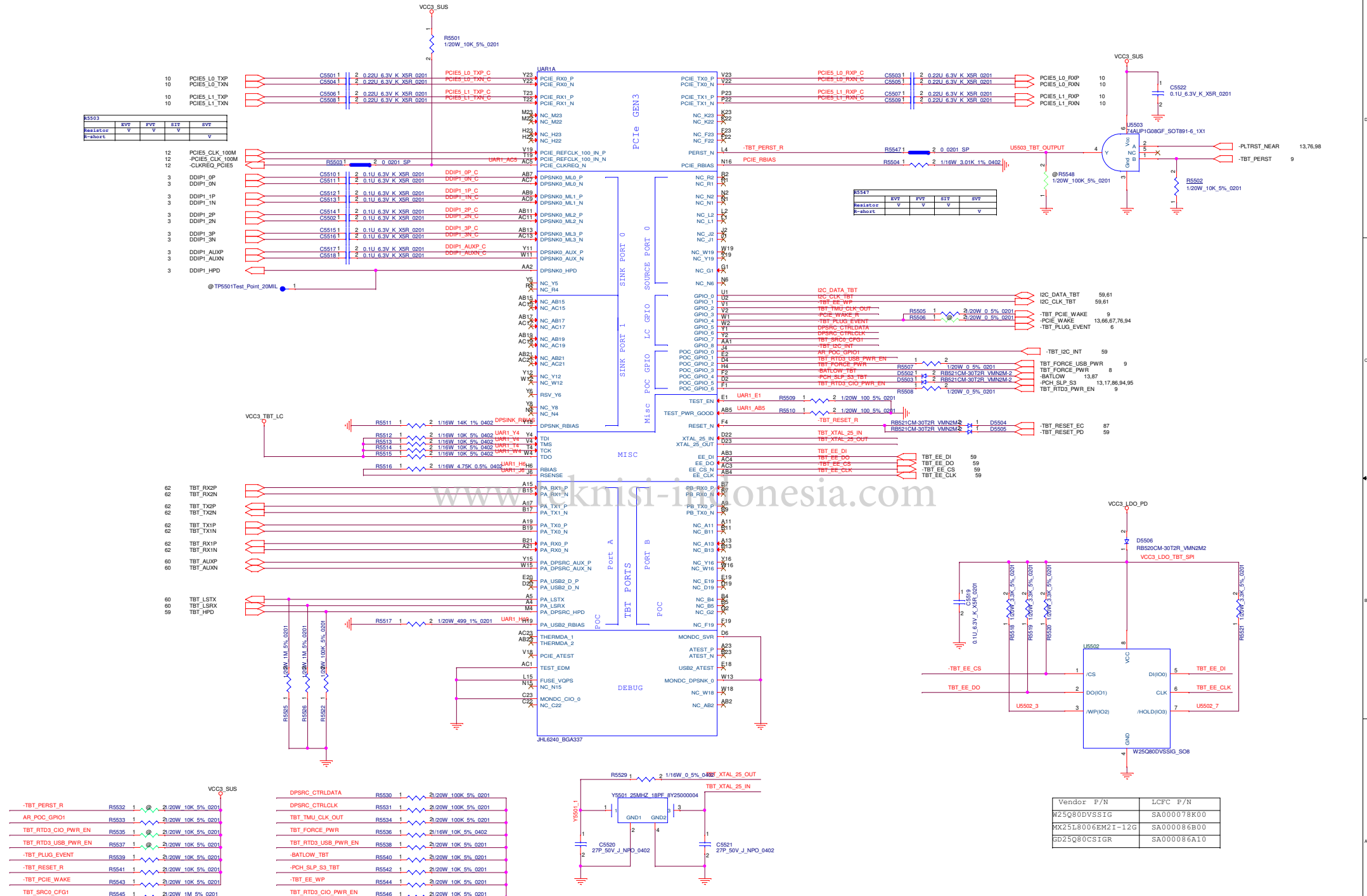
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2018/01/12		2018/01/12			
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				C	
				Jazz/Sideswipe	
Date:				Friday, December 28, 2018	Sheet 53 of 125



DESIGN	REV	DATE	BY	CHK
DESIGN	1	2018/01/12	LC	LC
REV	1	2018/01/12	LC	LC



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-TBT_PERST_R	R5532	1	2/20W 10K 5% 0201
AR_POC_GPI01	R5533	1	2/20W 10K 5% 0201
TBT_RT03_CIO_PWR_EN	R5535	1	2/20W 10K 5% 0201
TBT_RT03_CIO_PWR_EN	R5537	1	2/20W 10K 5% 0201
-TBT_PLUG_EVENT	R5539	1	2/20W 10K 5% 0201
-TBT_RESET_R	R5541	1	2/20W 10K 5% 0201
-TBT_POW_WAKE	R5543	1	2/20W 10K 5% 0201
TBT_SRC0_CFG1	R5545	1	2/20W 1M 5% 0201

DPSRC_CTRLCLK	R5530	1	2/20W 100K 5% 0201
DPSRC_CTRLCLK	R5531	1	2/20W 100K 5% 0201
TBT_TMU_CLK_OUT	R5534	1	2/20W 100K 5% 0201
TBT_FORCE_PWR	R5536	1	2/18W 10K 5% 0402
TBT_RT03_USB_PWR_EN	R5538	1	2/20W 10K 5% 0201
-BATLOW_TBT	R5540	1	2/20W 10K 5% 0201
-PCH_SLP_S3_TBT	R5542	1	2/20W 10K 5% 0201
-TBT_EE_WP	R5544	1	2/20W 10K 5% 0201
TBT_RT03_CIO_PWR_EN	R5546	1	2/20W 10K 5% 0201

Vendor	P/N	LCFC P/N
TXC	8Y25000004	SJ10000H00J
KDS	1ZZHAE25000CC0F	SJ10000P300

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Vendor P/N	LCFC P/N
W25Q80DVSSIG	SA000078K00
MX25LI006EM2I-12G	SA000086B00
SD25Q80CSIGR	SA000086A10

ALPINE RIDGE (1/2)

Jazz/Sideswipe

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				Sheet	Rev
				Date:	Friday, December 28, 2018
				Sheet	97 of 125



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Date:	Friday, December 28, 2018 (Sheet 58 of 125)				

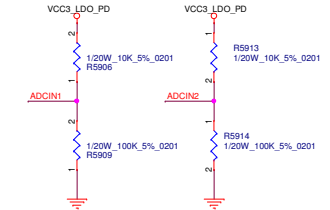
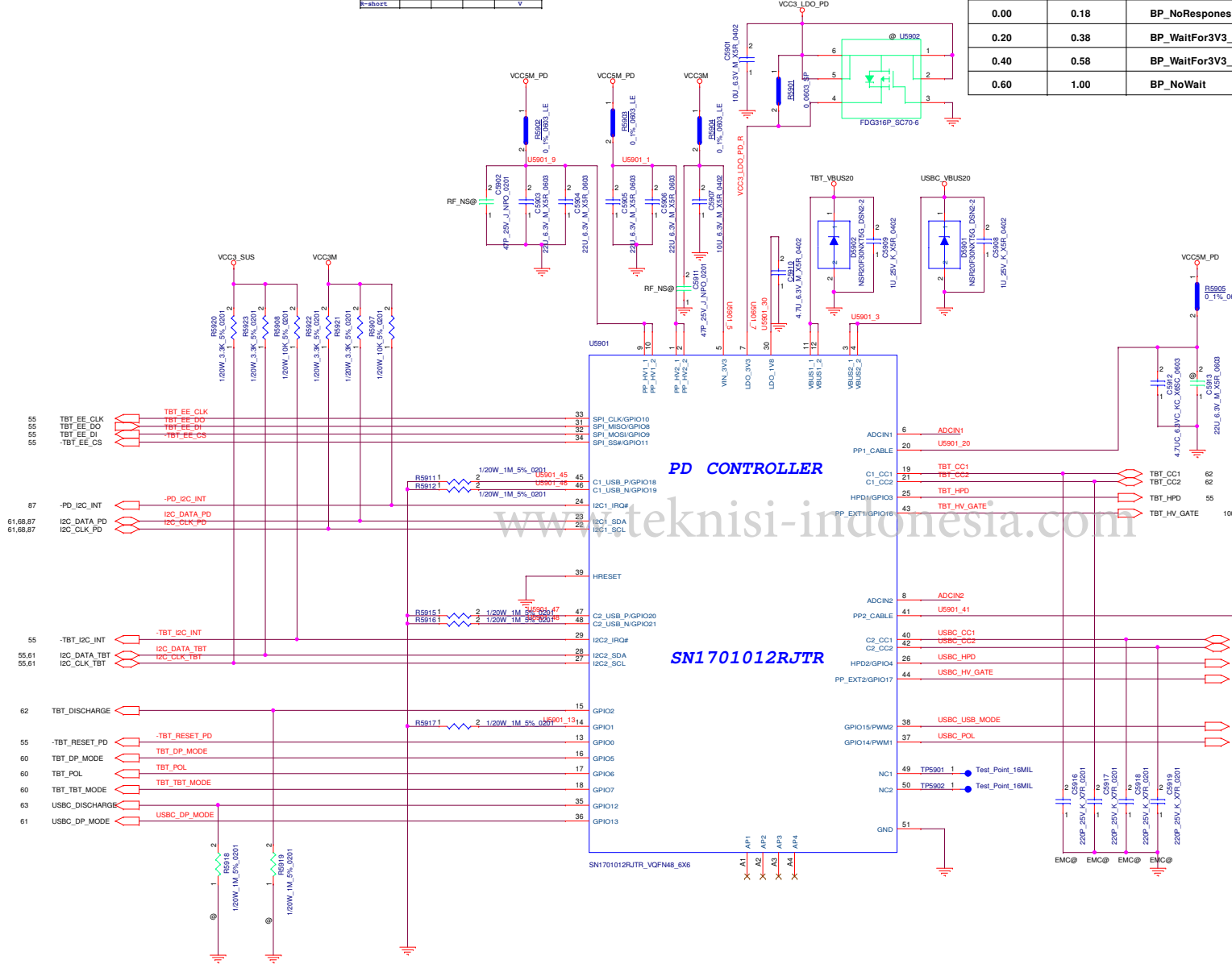
R5901, R5902, R5903, R5904				
Resistor	5V1	5V2	5V1	5V1
0-Short	V	V	V	V

TABLE BUSPOWER Configuration - ADCIN1

DIV = R2/ (R1+R2)		Configuration
DIV MIN	DIV MAX	
0.00	0.18	BP_NoResponses
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

TABLE BUSPOWER Configuration - ADCIN2

DIV = R2/ (R1+R2)		I2C Unique Address [3:1]	
DIV MIN	DIV MAX	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b



R5905, R5910				
Resistor	5V1	5V2	5V1	5V1
0-Short	V	V	V	V

R6003, R6001, R6004				
RVF	PVF	SVF	SVF	
Resistor	V	V	V	V
Resistor	V	V	V	V

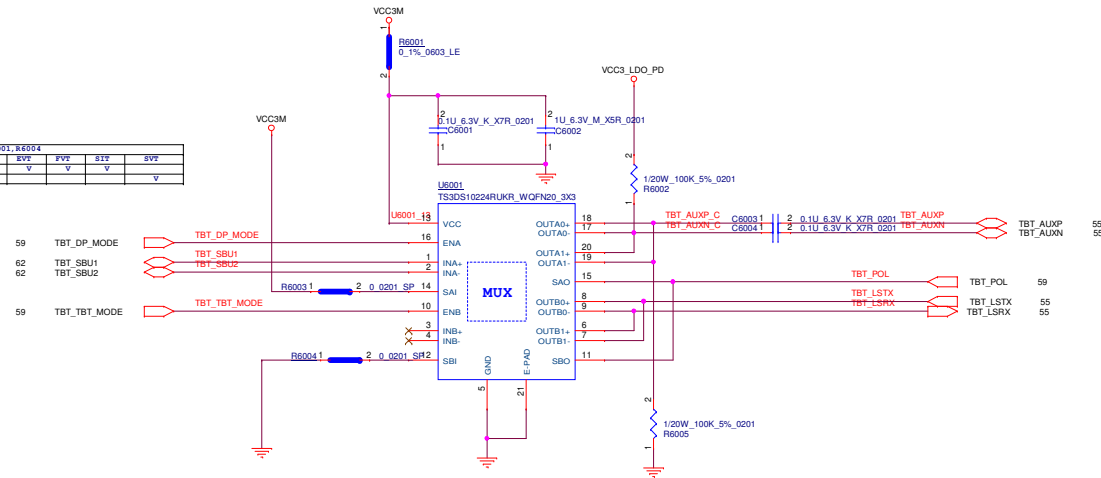
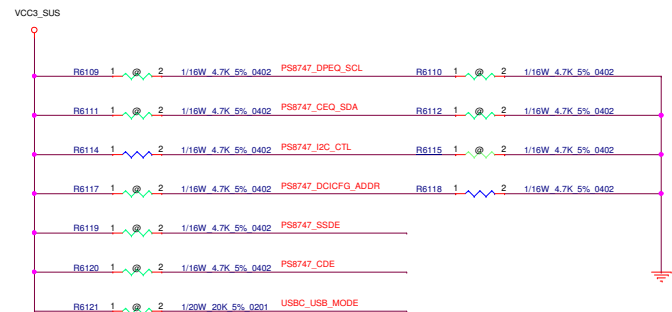
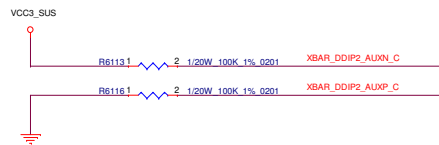
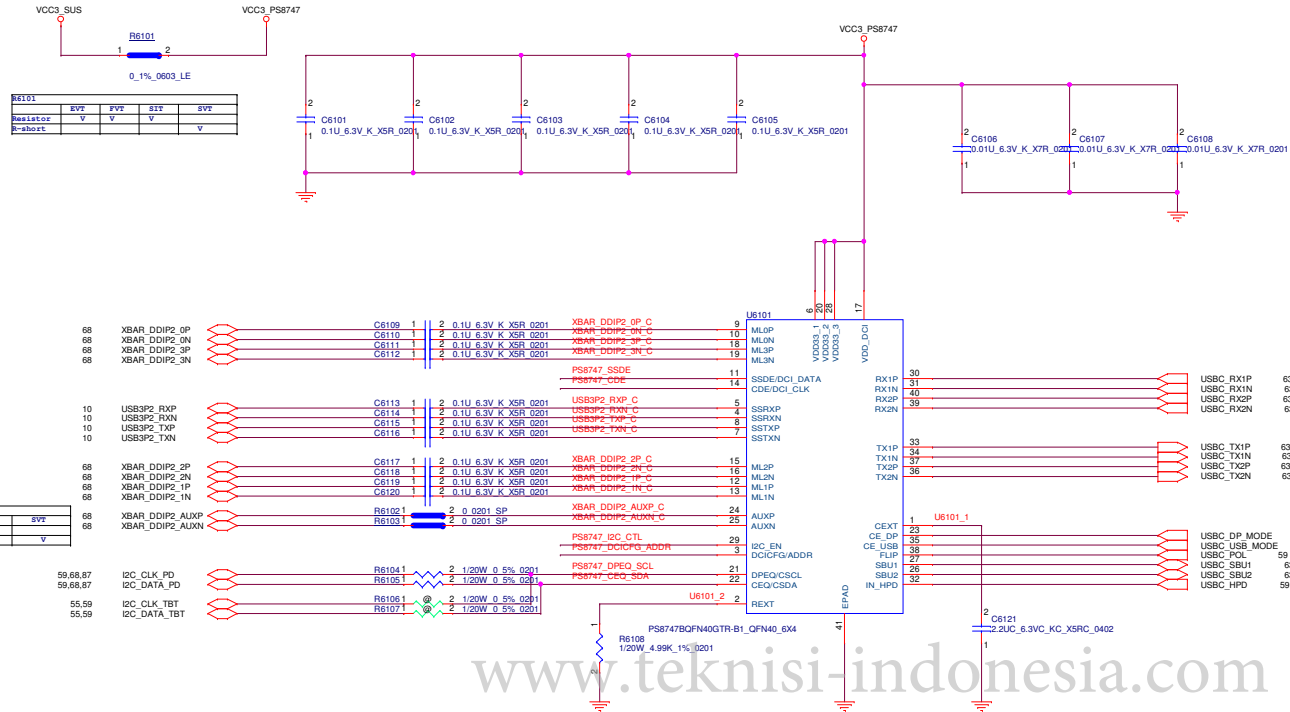
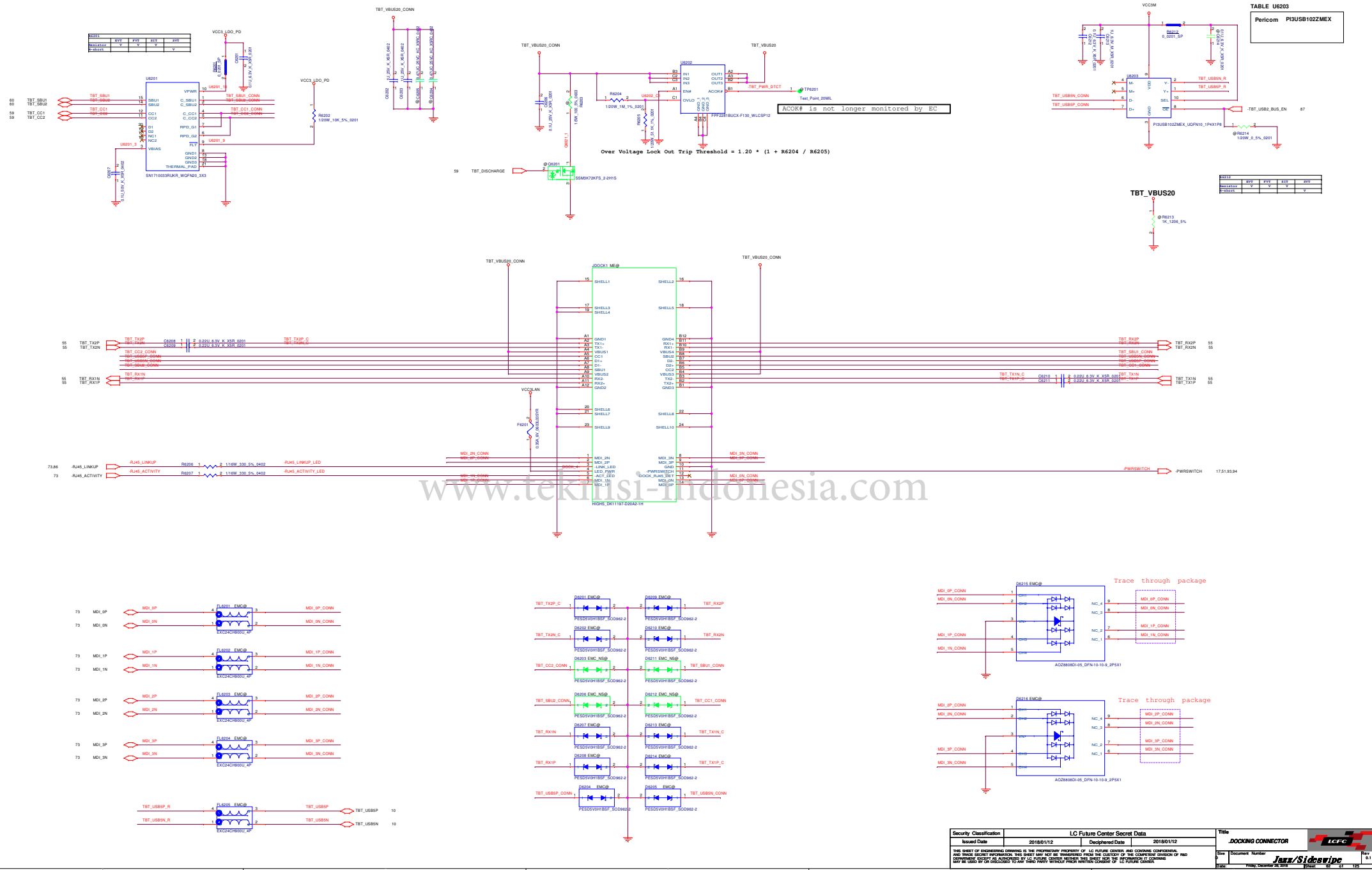
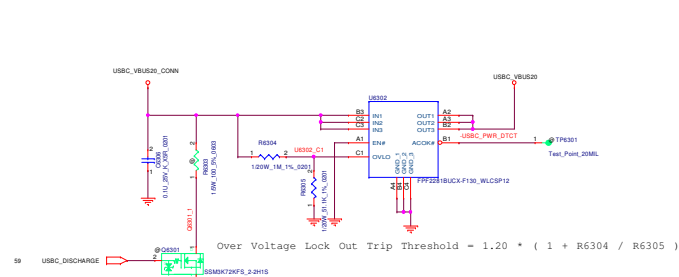
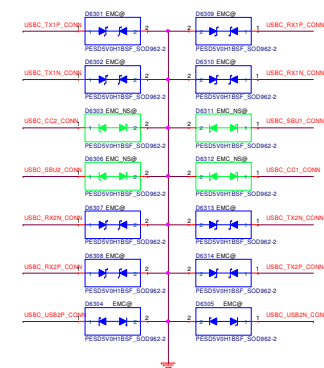


TABLE of U6001		
Vendor	P/N	LCFC P/N
TI	TS3DS10224RUKR	SA00008AS00
DIODES	PI3DBS3224ZNAEX	SA00008CC00

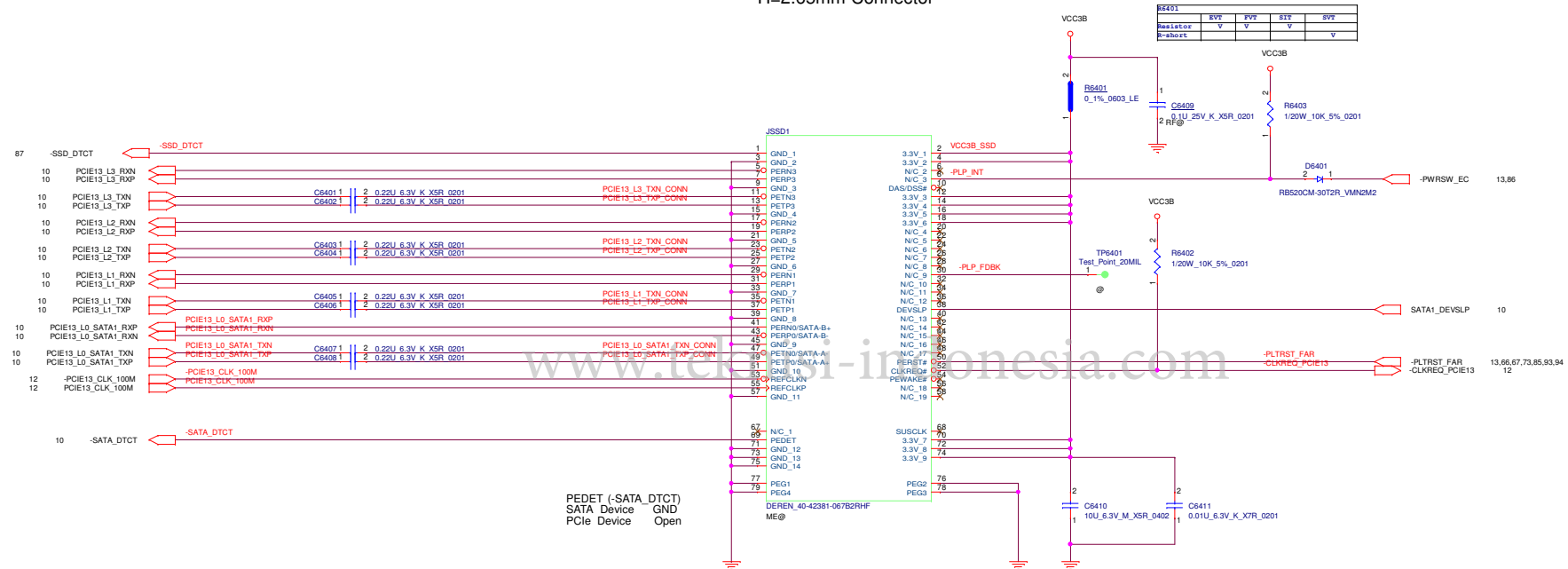




[illegible]


M.2 Socket 3 (Key-M) for 2280 S3 SSD

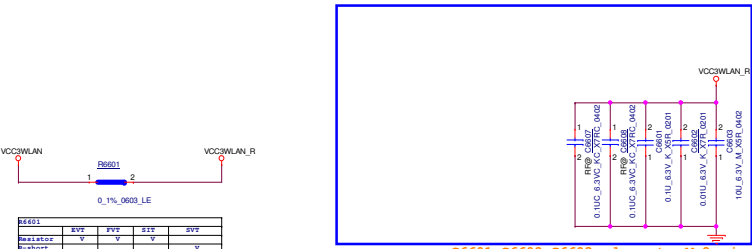
H=2.65mm Connector



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Custom		Jazz/Sideswipe		Friday, December 28, 2018		0.1
				Sheet		69 of 129



R6601	RVE	RVE	RVE	RVE
1	V	V	V	V
2	V	V	V	V

C6601,C6602,C6603 close to M.2 pin 4 and pin5

C6604,C6605,C6606 close to M.2 pin72 and pin73

TABLE

Companion RF (CRF)	CNVio	REFCLK	CLKREQ
Jefferson Peak (JfP)	Gen1	Supported	Supported
Harrison Peak (HrP)	Gen2	Not Supported	Not Supported

TABLE

Platform	CNVio	PCH IP	REFCLK
Whiskey Lake	Gen1	Pulsar	38.4MHz Clock form JfP Module
Ice Lake	Gen2	Quasar	Generated inside SoC

M.2 Type 1216 Module for WLAN / Bluetooth

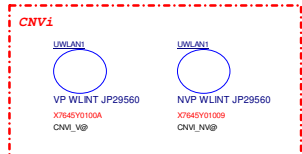
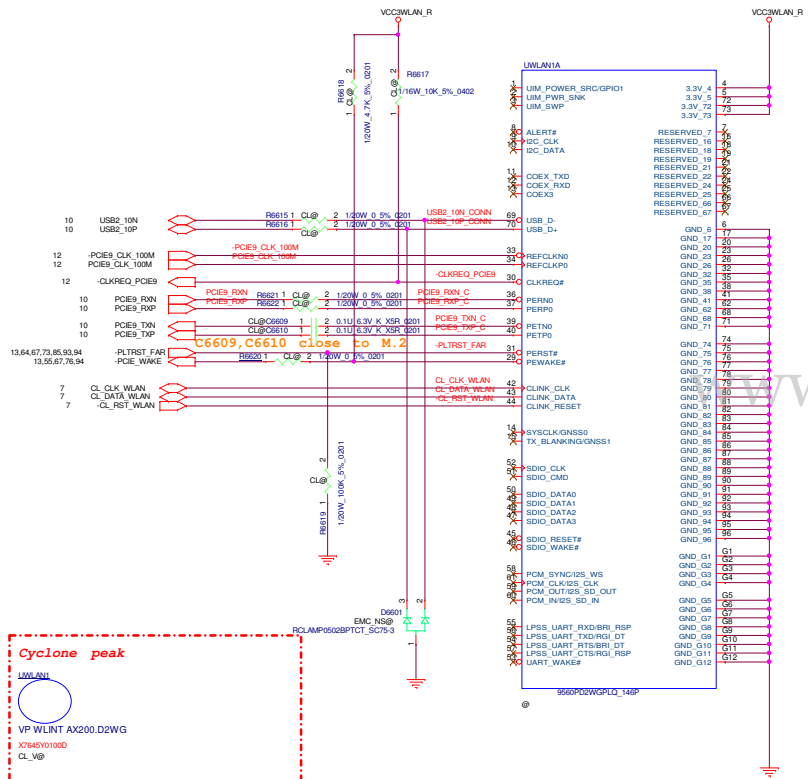
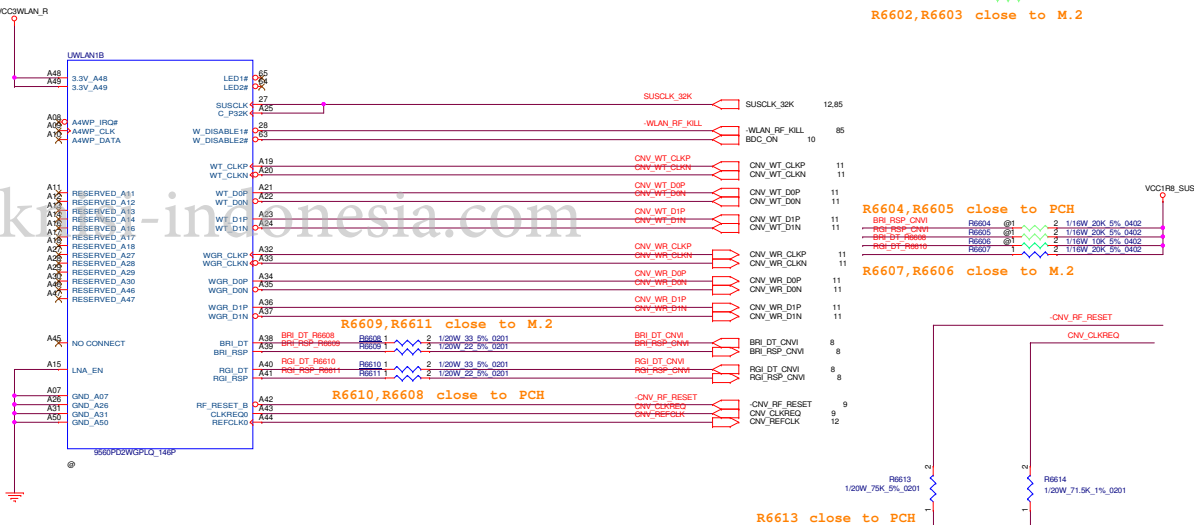


TABLE of CNV1 (UWLAN1A & UWLAN1B)

Vendor	Model	LCFC P/N
Intel	Intel Jefferson Peak 2 9560 2*2ac+BT5.0 vPro M.2 1216 LGA	PK29S001400
Intel	Intel Jefferson Peak 2 9560 2*2ac+BT5.0 non-vPro M.2 1216 LGA	PK29S001500



R6613 close to PCH

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Rev	0.1	Document Number	Jaxx/Sideswipe
Date	Friday, December 28, 2018	Sheet	68 of 126

M.2 Socket 2 (Key-B) for 3042 S3 WWAN

H=2.00mm Connector

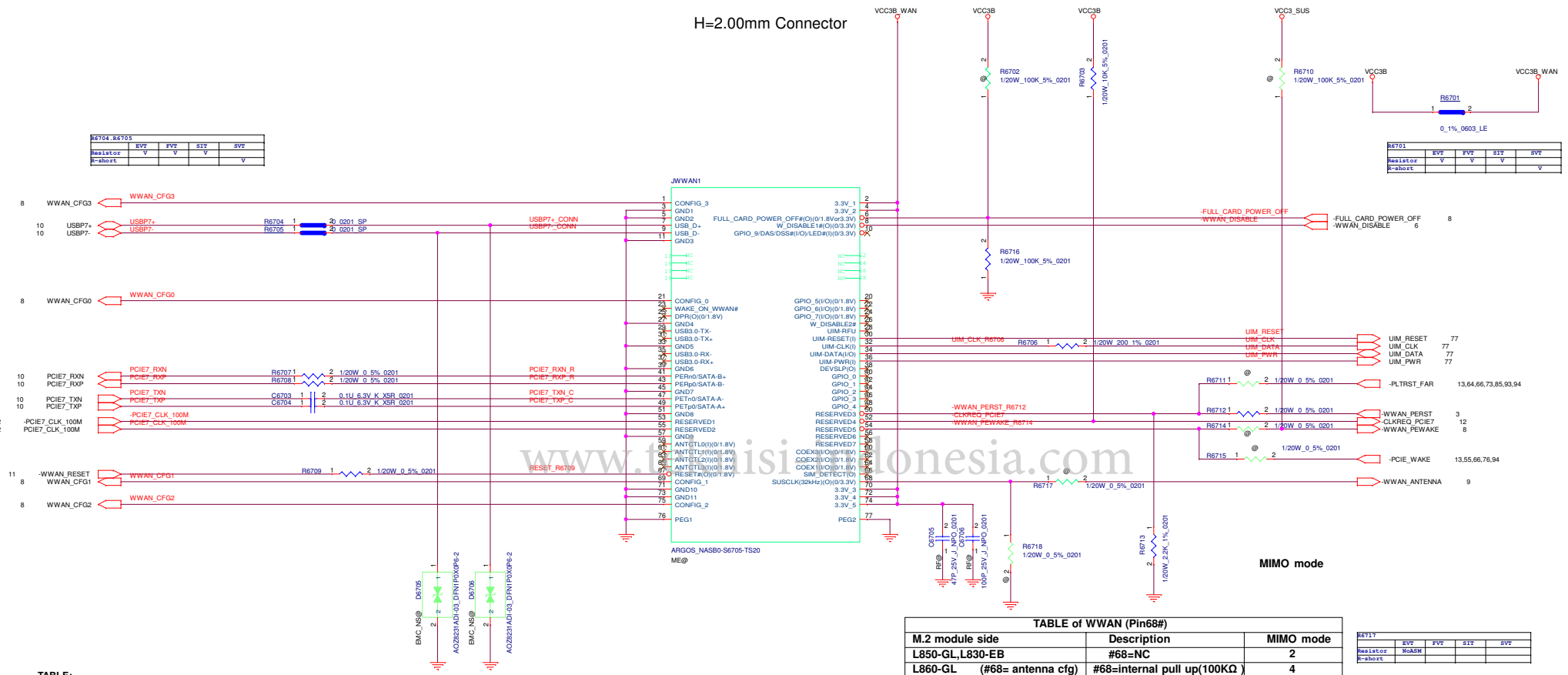


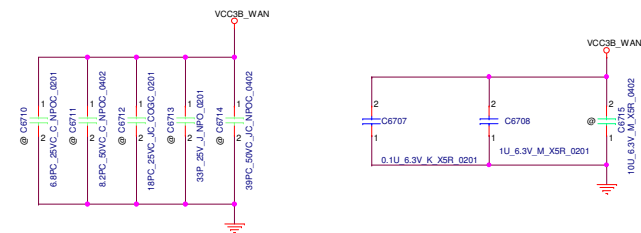
TABLE of WWAN (Pin68#)



M.2 module side	Description	MIMO mode
L850-GL,L830-EB	#68=NC	2
L860-GL (#68= antenna cfg)	#68=internal pull up(100KΩ)	4

R6717				
	EVT	FVT	SIT	SVT
Resistor	NoASM			
R-short				

TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration	Module
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)			
0	GND	GND	GND	GND	SSD - SATA	N/A	
1	GND	GND	GND	NC	SSD - PCIe	N/A	
2	GND	GND	NC	GND	WWAN - PCIe	0	
3	GND	GND	NC	NC	WWAN - PCIe	1	WWAN L850
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0	
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1	
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2	
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3	WWAN L830
8	NC	GND	GND	GND	WWAN - SSIC	0	
9	NC	GND	GND	NC	WWAN - SSIC	1	
10	NC	GND	NC	GND	WWAN - SSIC	2	
11	NC	GND	NC	NC	WWAN - SSIC	3	
12	NC	NC	GND	GND	WWAN - PCIe	2	
13	NC	NC	GND	NC	WWAN - PCIe	3	
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined	WWAN L860
15	NC	NC	NC	NC	No Module Present	N/A	



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				Date:	Friday, December 28, 2018	Sheet 97 of 120	

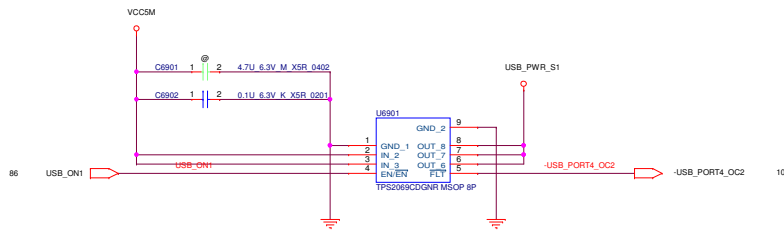
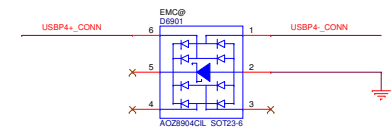
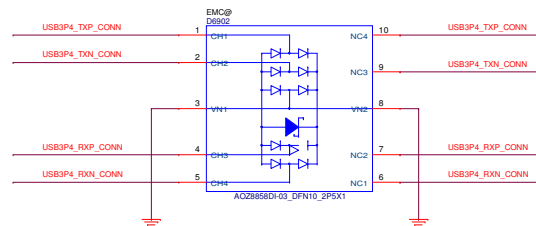
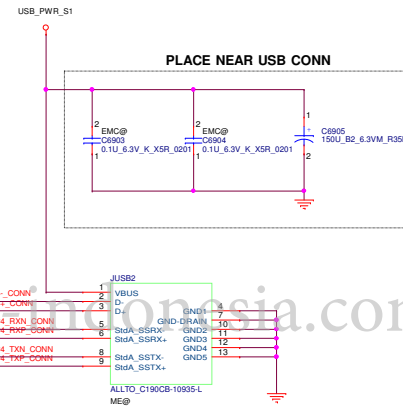
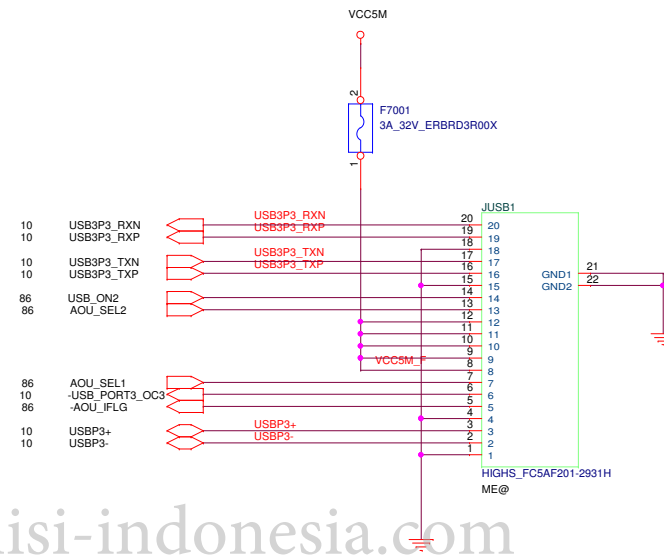


TABLE of USB3.0 Single (U6901)		
Vendor	P/N	LCFC P/N
TI	TPS2069CDG9R	SA00005TE00
Rohm	BD82032FVJ-GE2	SA000084S00

	SVF	PVZ	SVF	SVF
DC/DC	V			
Regulator				






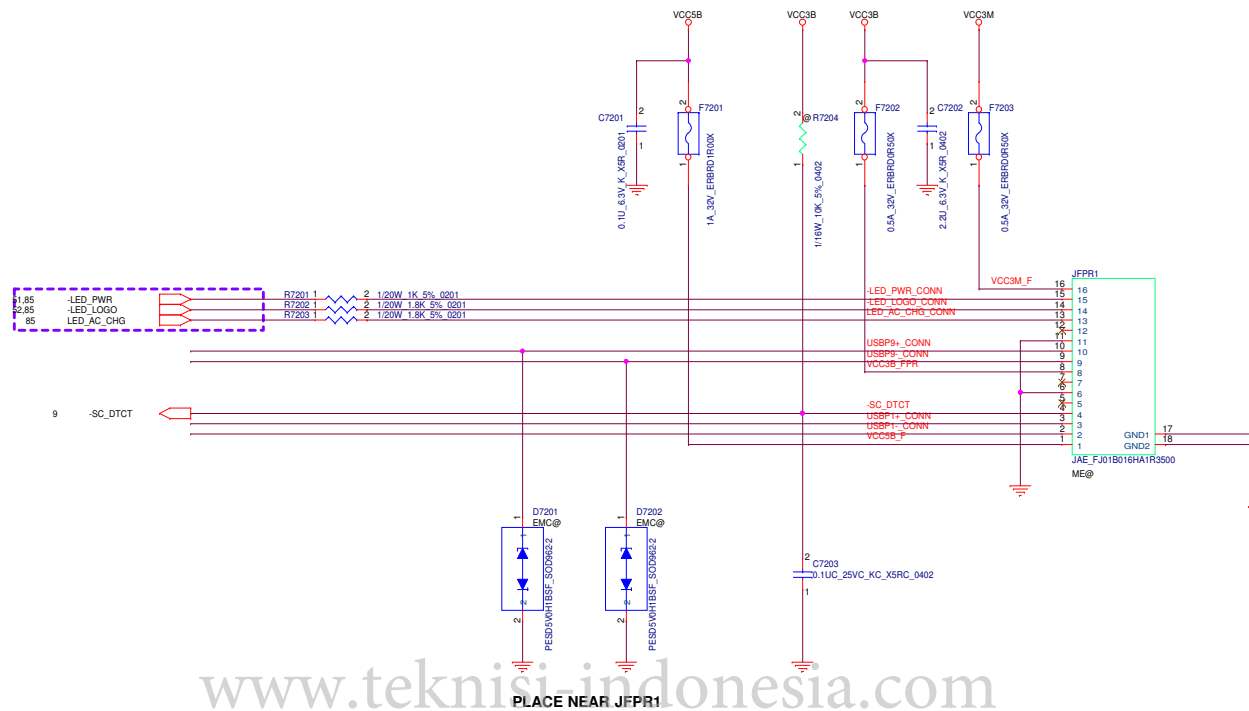
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				Custom		Friday, December 28, 2018	
				Jazz/Sideswipe		Sheet 71 of 126	

For NEC LED



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PLACE NEAR JFPR1

For FPR

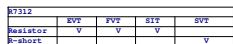


PLACE NEAR JFPR1

For Smart card



R7205, R7206, R7207, R7208	SIZE	VALUE	UNIT	TYPE
Resistor	V	V	V	V
R-short				



R7314				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

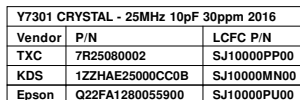
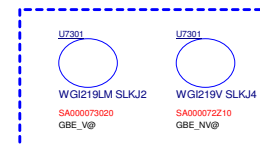


TABLE		
0201	vPro	Capability
GbE PHY	Yes	No
U7301	Jacksonville-LM	Jacksonville-V


↑
LOGIC




SKU	Description	LCFC P/N
vPRO	WGI219LM SLKJ2	SA000073020
non-vPRO	WGI219V SLKJ4	SA000072210

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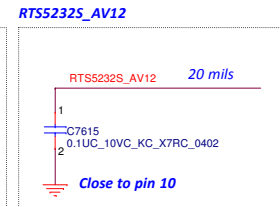
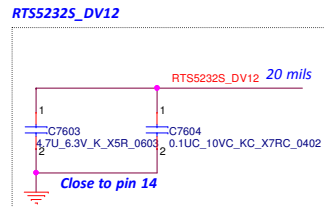
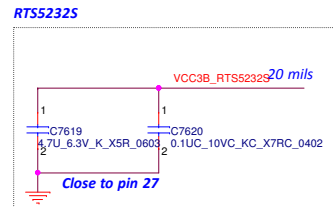
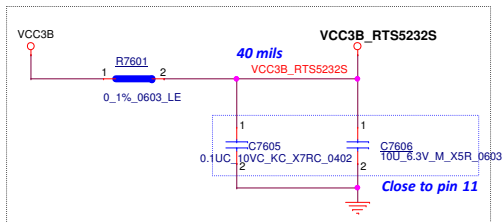
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Date: Friday, December 28, 2018				Sheet: 74 of 129	Rev: 0.1



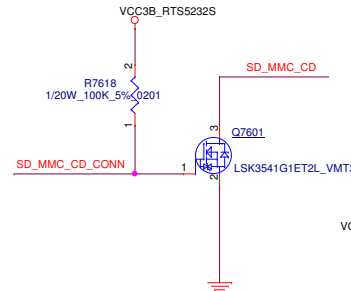
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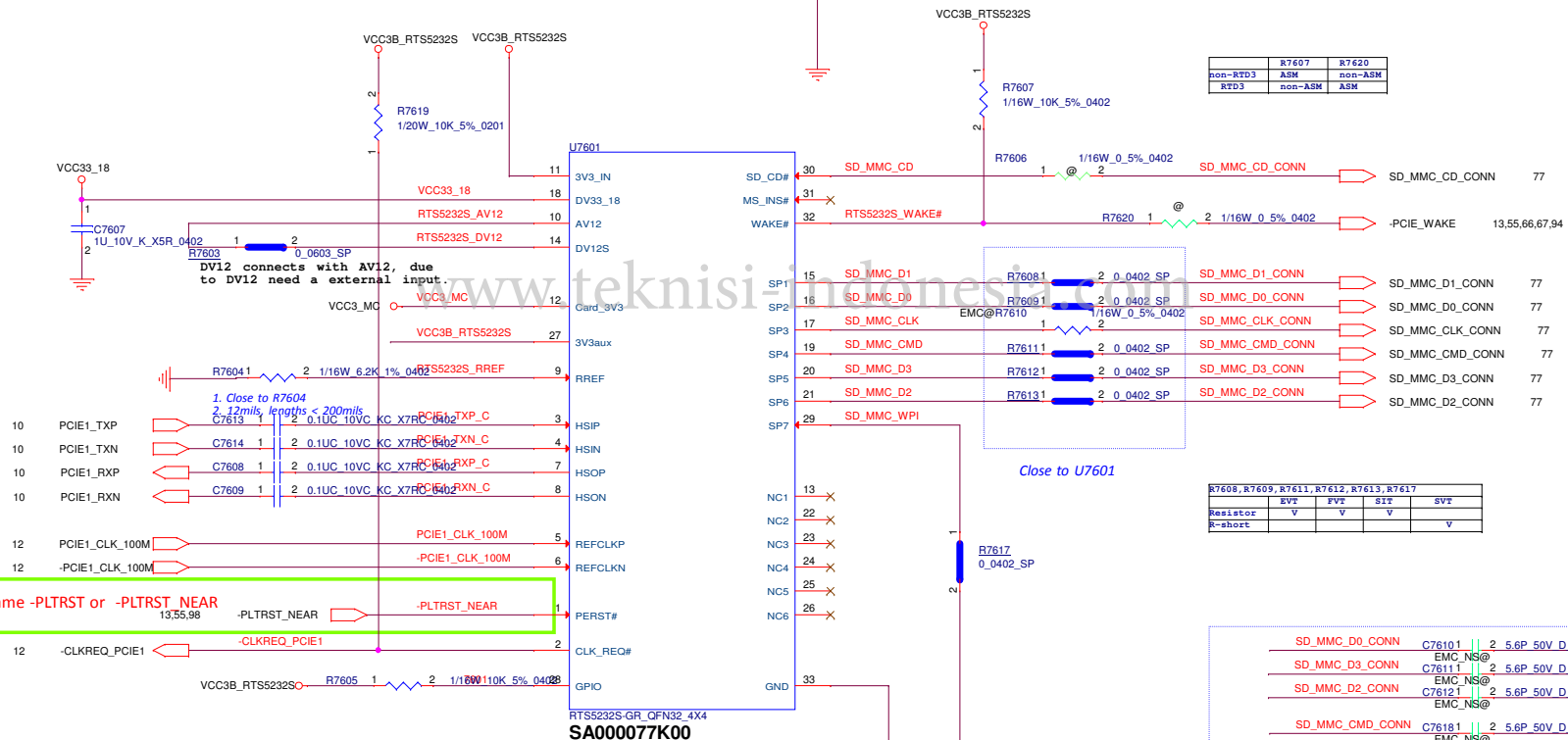
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Date: Friday, December 28, 2018					Sheet	79	of	129



R7601, R7603				
EVT	FVT	SIT	SVT	
Resistor	V	V	V	V
K-short				



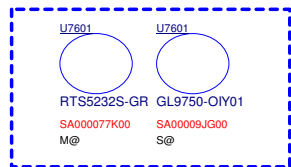
	R7607	R7620
non-RTD3	ASM	non-ASM
RTD3	non-ASM	ASM



	R7608	R7609	R7611	R7612	R7613	R7617
EVT	V	V	V	V	V	V
FVT	V	V	V	V	V	V
SIT	V	V	V	V	V	V
SVT	V	V	V	V	V	V
K-short						

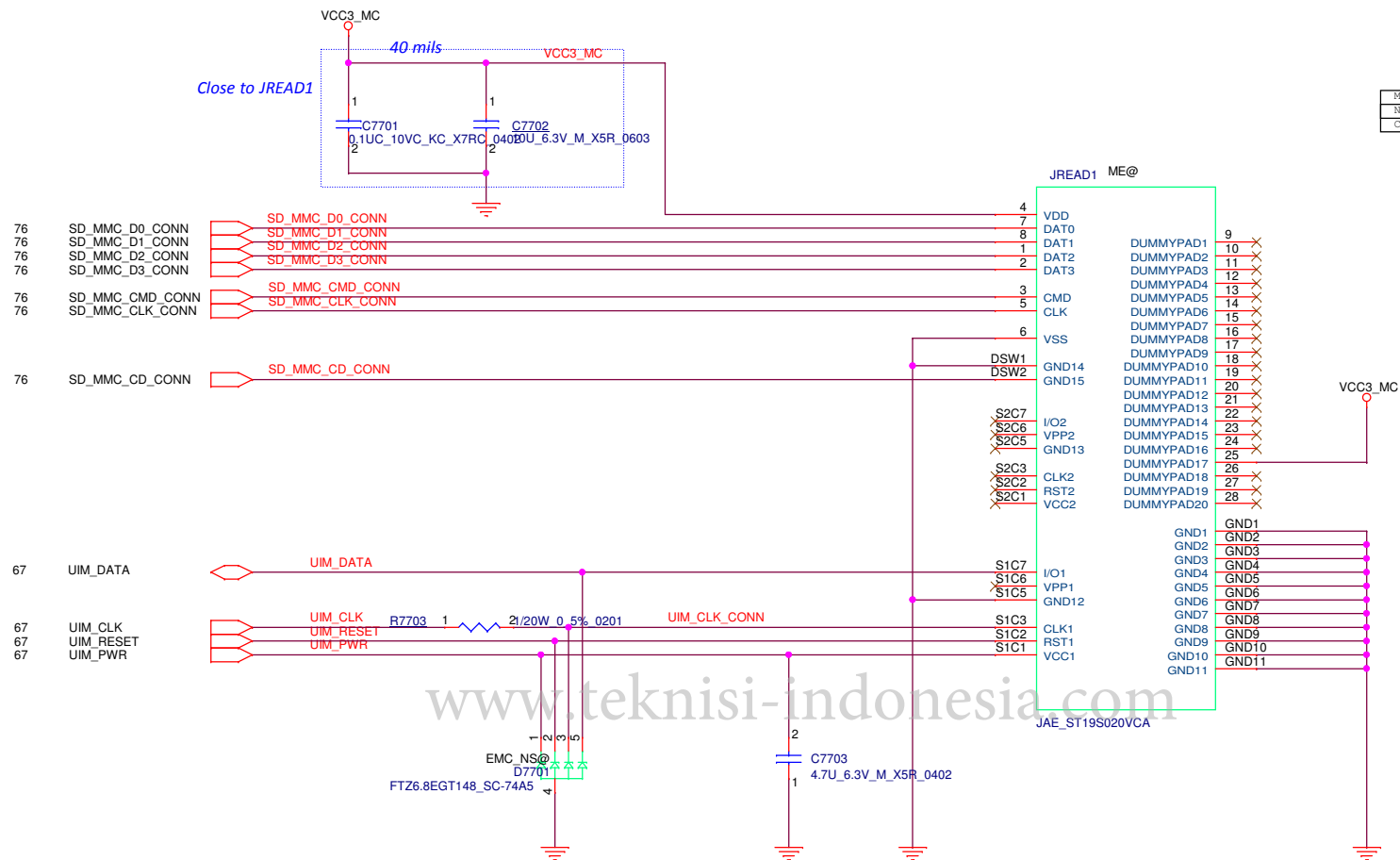
Check inet name -PLTRST or -PLTRST_NEAR
13,55,98 -PLTRST_NEAR -PLTRST_NEAR
12 -CLKREQ_PCIE1 -CLKREQ_PCIE1

Part Number	Vendor
SA000077K00	RTS5232S-GR REALTEK
SA00009JG00	GL9750-OIY02 GENESYS




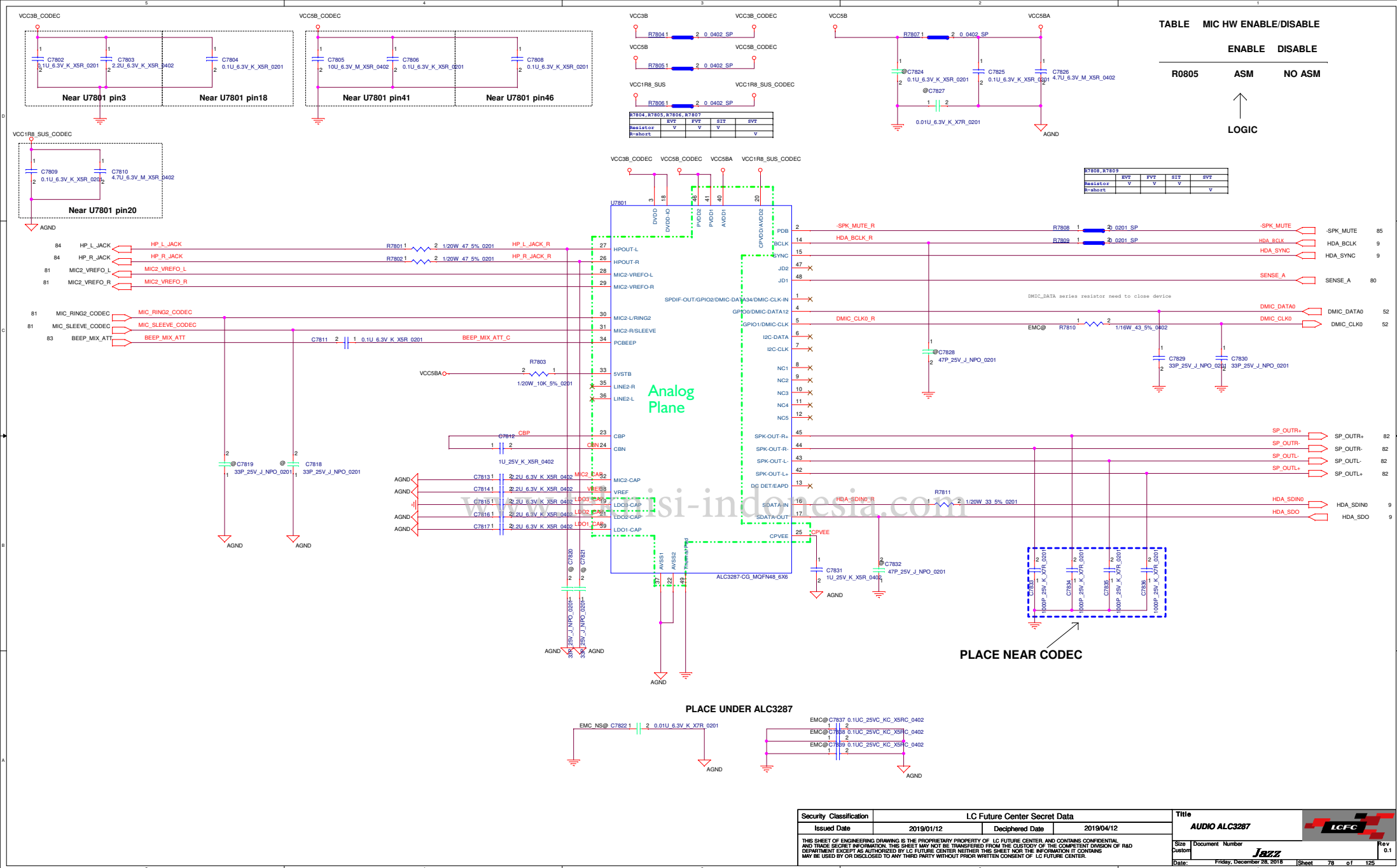
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Issued Date	2019/01/12
Deciphered Date	2019/04/12
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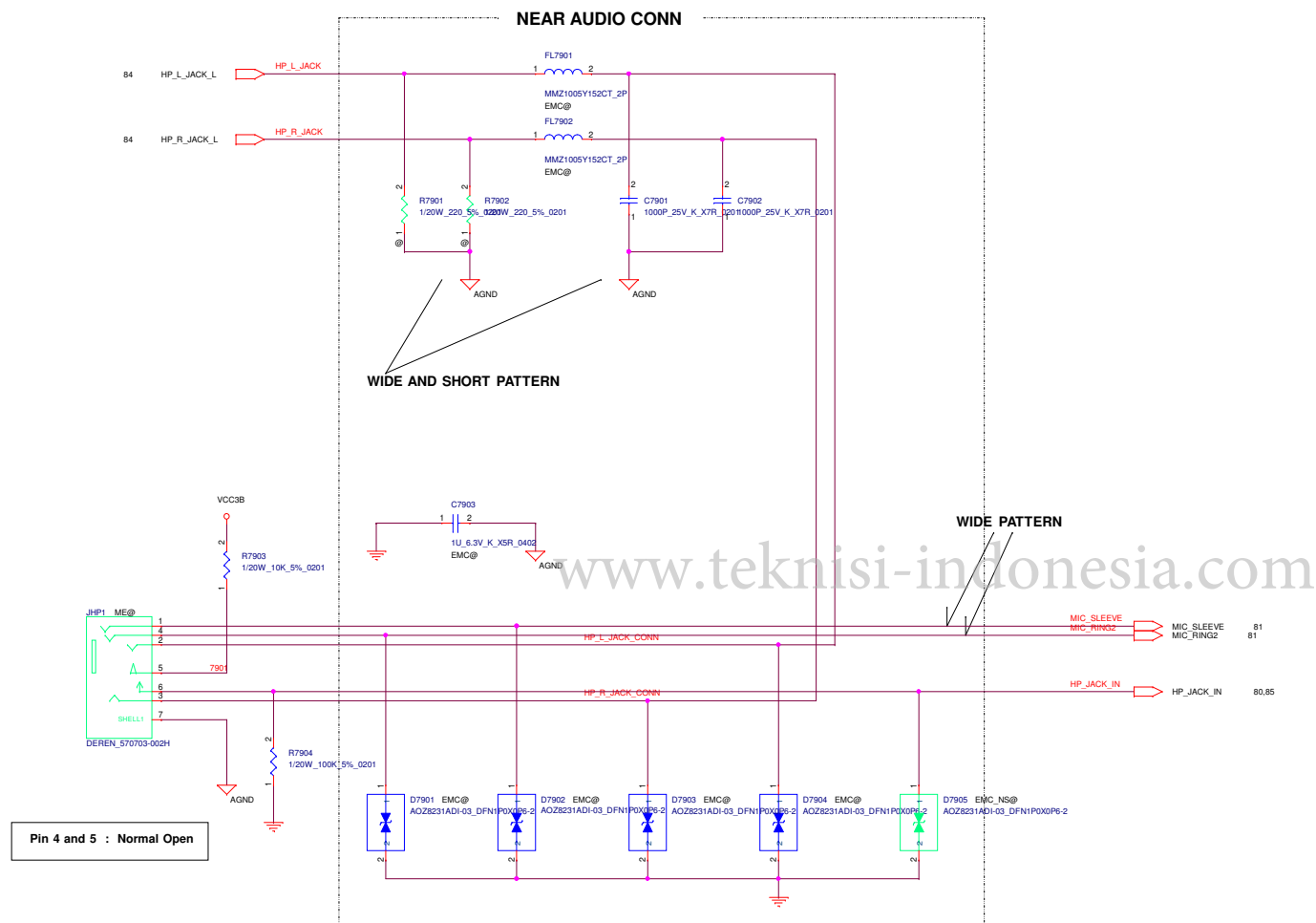
Title	MEDIA CARD CONTROLLER
Size	Custom
Document Number	T49087590
Date	Thursday, January 03, 2019
Sheet	76 of 125
Rev	0.1

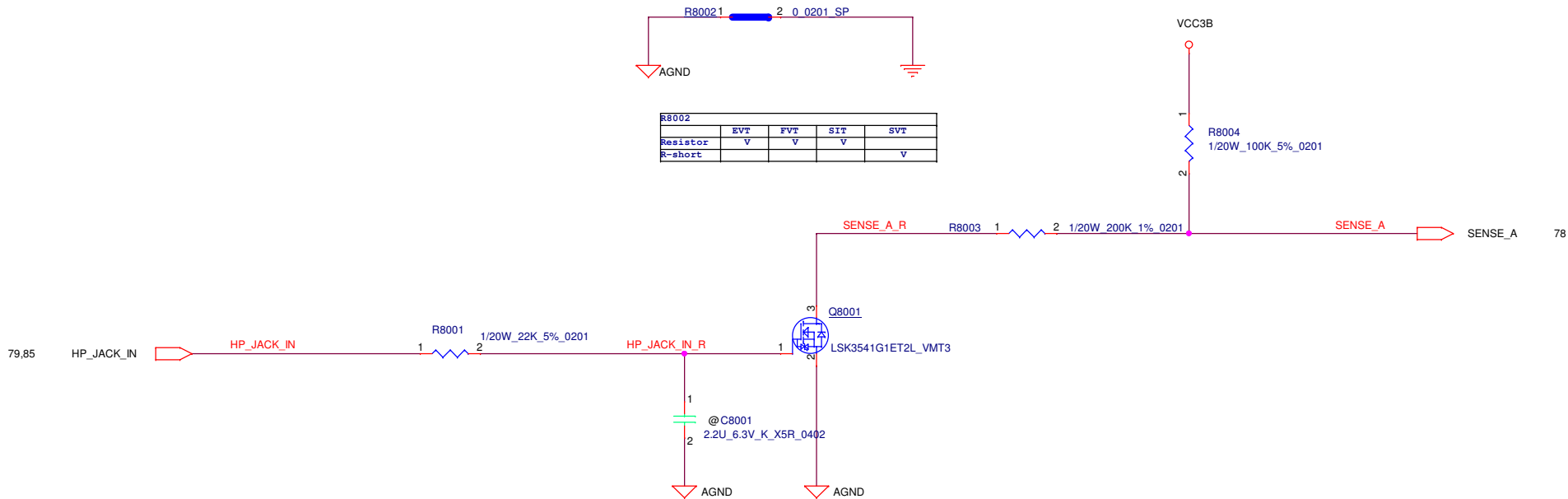


Mode	Detect
Normal	short
Card Insert	open

Security Classification		LC Future Center Secret Data				Title MEDIA CARD CONTROLLER			
Issued Date		2019/01/12		Deciphered Date					
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Size		Document Number		T490&T590				Rev	
B								0.1	
Date:		Friday, December 28, 2018		Sheet		77 of		125	

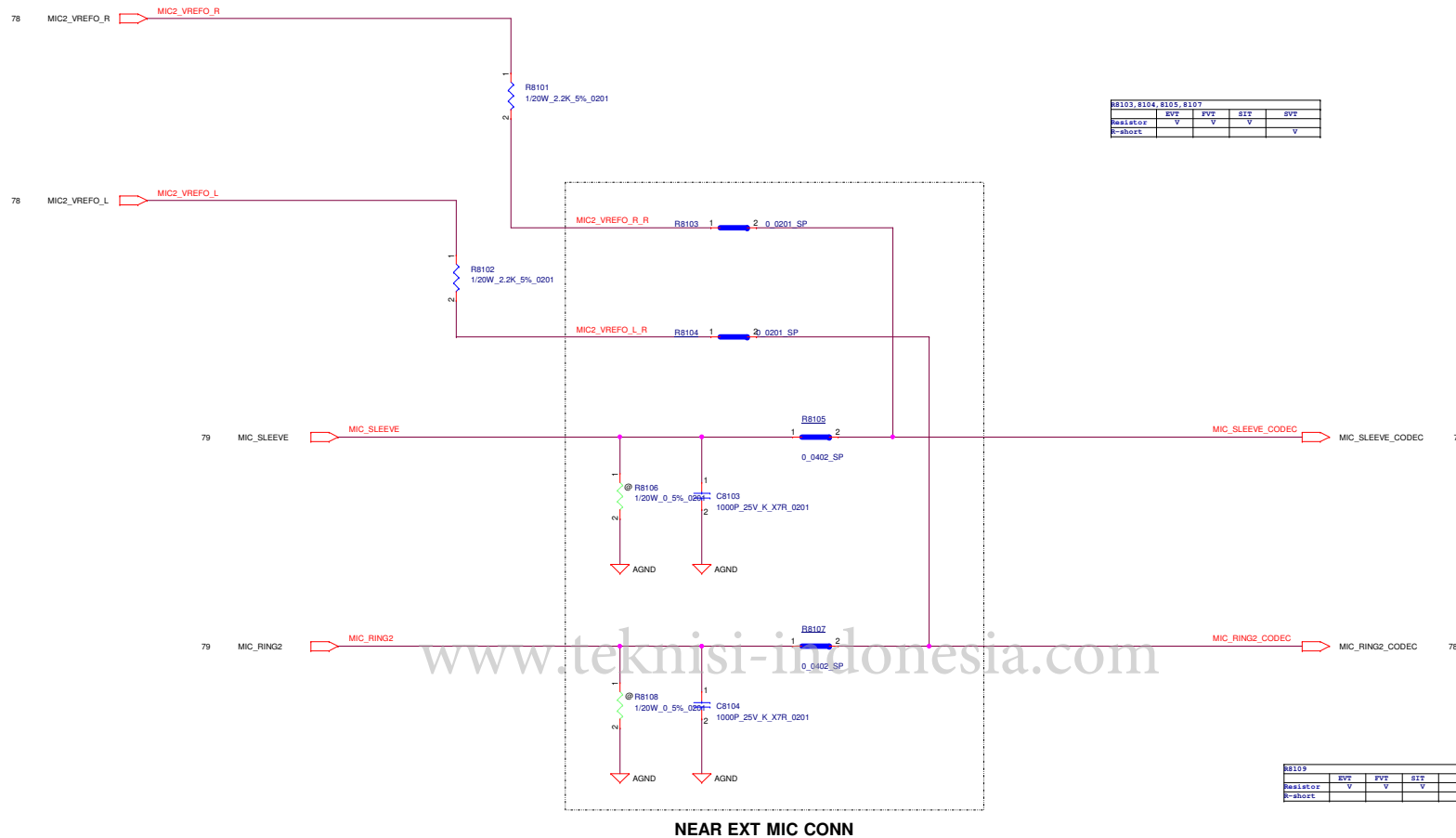






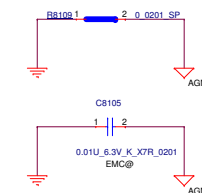
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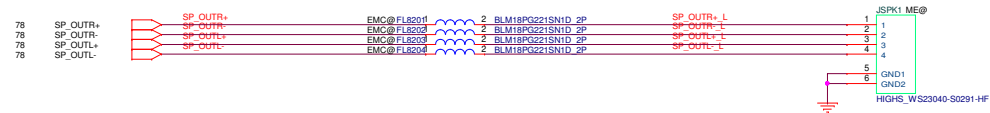
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Issued Date	2019/01/12	Deciphered Date	2019/04/12	AUDIO JACK SENSE	
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				Jazz	
				Date:	Friday, December 28, 2018
				Sheet	80 of 125
				Rev	0.1



R8103, R8104, R8105, R8107	SVF	SVF	SVF	SVF
Isolation	V	V	V	V
Re-shoot				V

R8109	SVF	SVF	SVF	SVF
Isolation	V	V	V	V
Re-shoot				V





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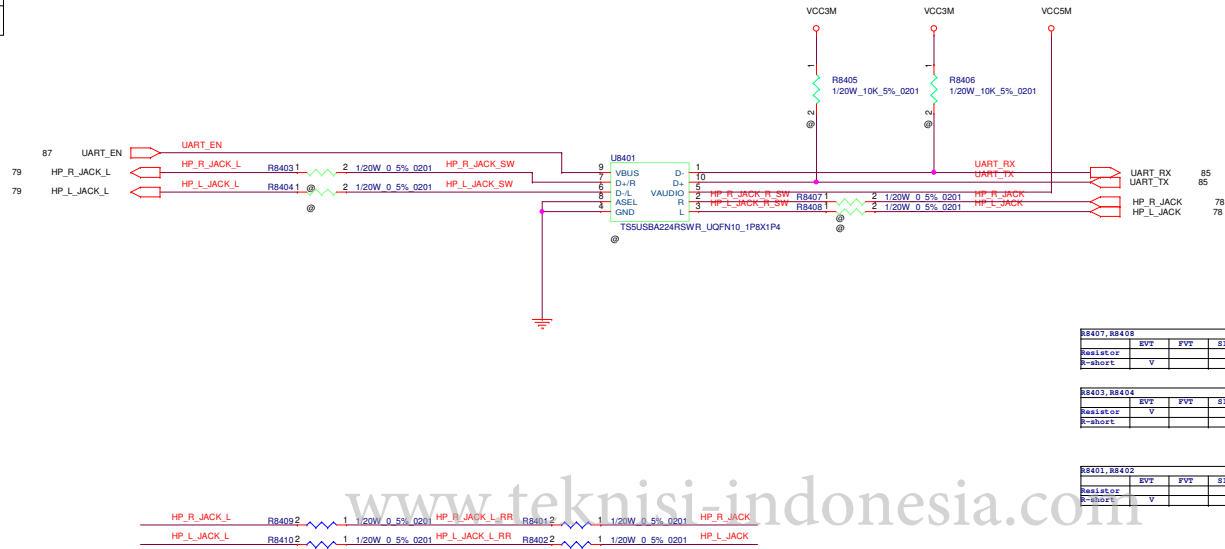
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Issued Date		Deciphered Date		AUDIO SPEAKER	
2019/01/12		2019/04/12			
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Size	Document	Number	Rev		0.1
C					
Date:	Friday, December 28, 2018		Sheet	82	of 125

TABLE:

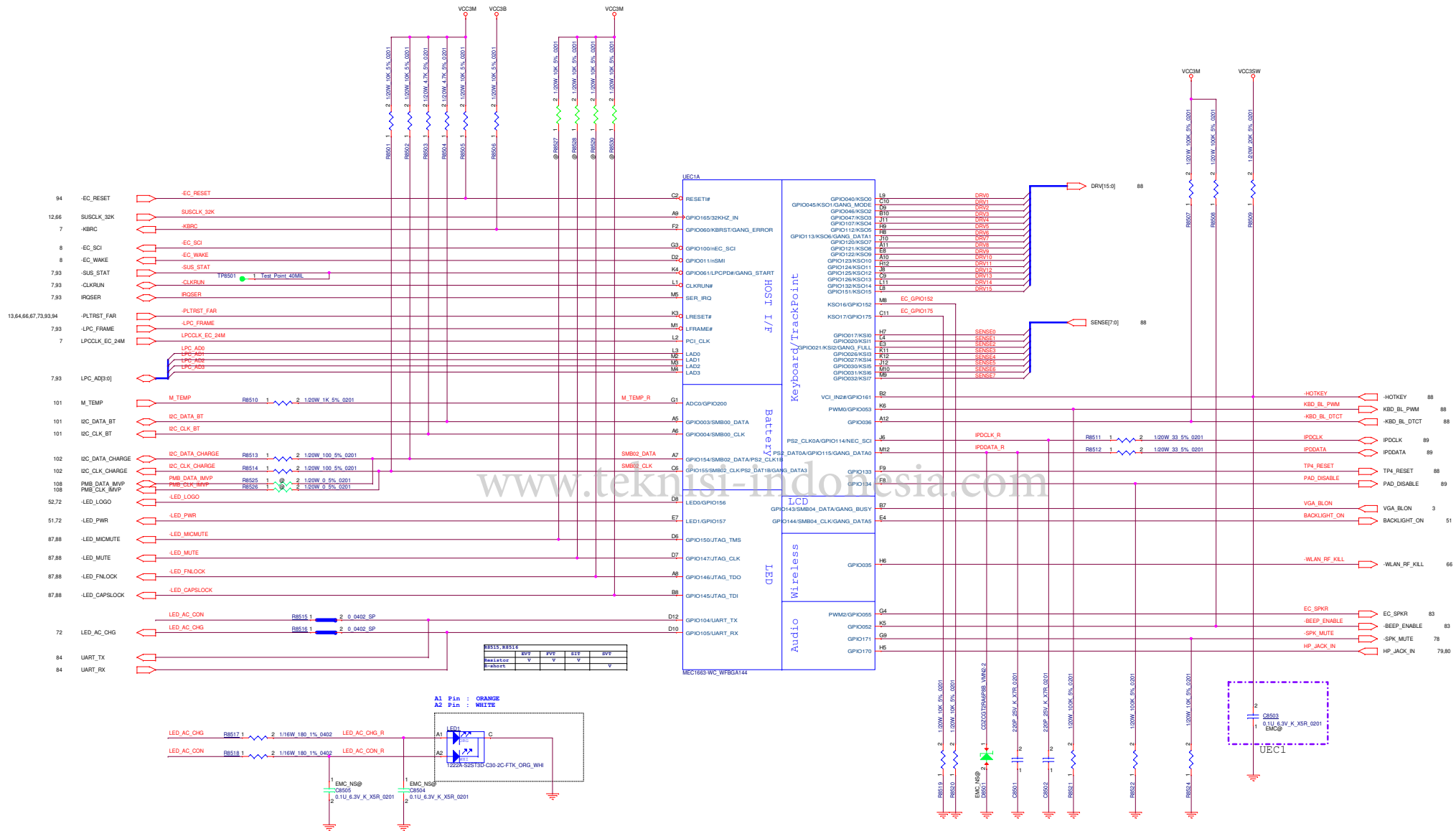
Mode	Audio	UART
UART_EN	L	H

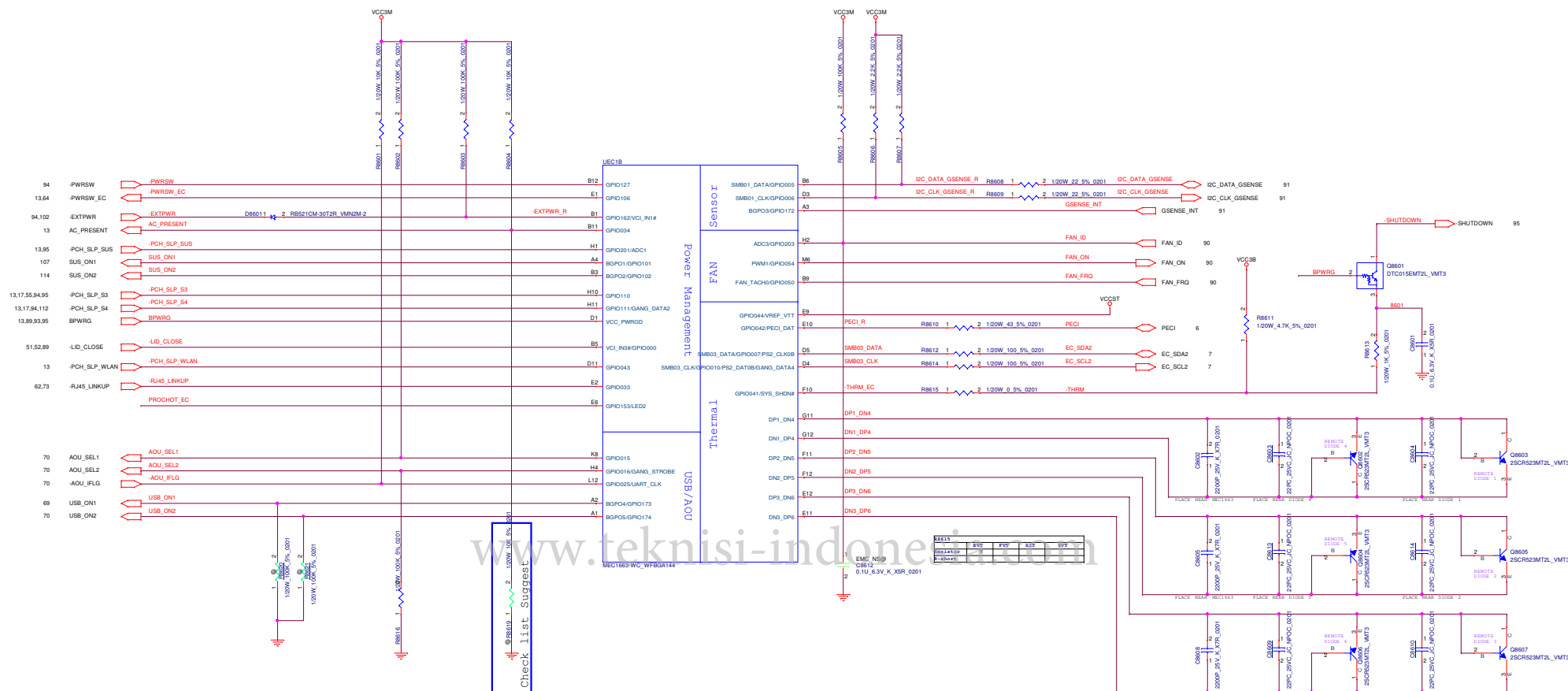


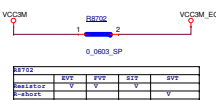
R8407, R8408	SVT	PVT	SIT	SVT
Result of	V			
R=MODE				

R8403, R8404	SVT	PVT	SIT	SVT
Result of	V			
R=MODE				

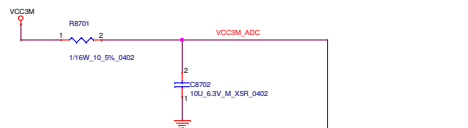
R8401, R8402	SVT	PVT	SIT	SVT
Result of	V			
R=MODE				







R702	V	V	V	V
R713/2/3	V	V	V	V
R713/2/3	V	V	V	V



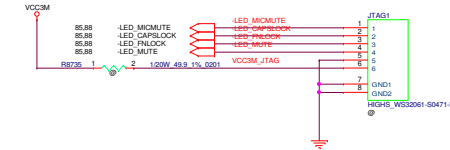
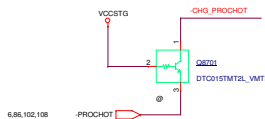
R713	V	V	V	V
R713/2/3	V	V	V	V
R713/2/3	V	V	V	V

- 94 ECSP_CLK
- 94 ECSP_MOSI
- 94 ECSP_MISO
- 94 ECSP_SS

3.51

9

6.8E102.108

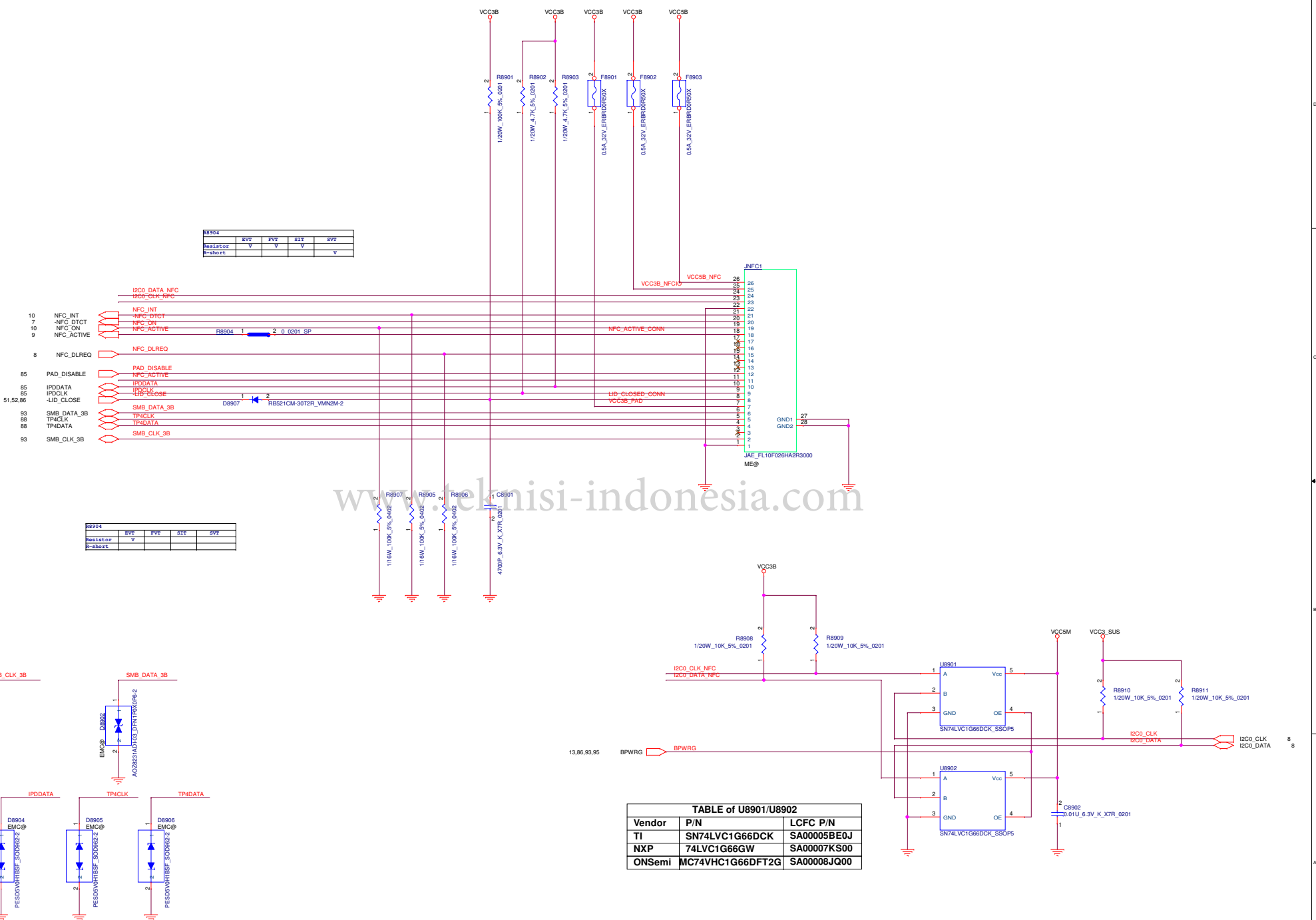


JTAG Debug Port		
	Enable	Disable
R8714	ASM	NO_ASM
R8715	NO_ASM	ASM
R8735	ASM	NO_ASM
R8527	ASM	NO_ASM
R8530	ASM	NO_ASM
R8529	ASM	NO_ASM
R8528	ASM	NO_ASM

Check list Suggest

H: DRIFT
L: JAZZ/SIDEWIRE

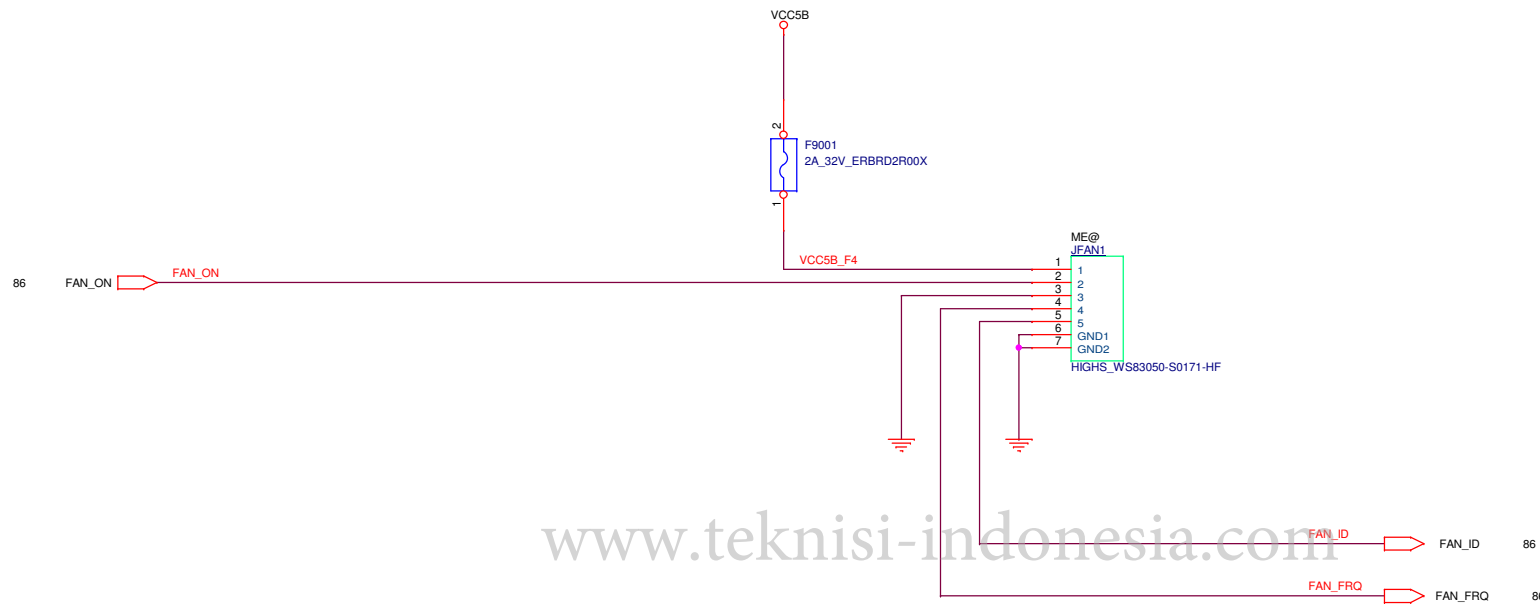




R8904				
Resistor	EV2	FV2	SV2	SV2
R-Short	V	V	V	V

R8904				
Resistor	EV2	FV2	SV2	SV2
R-Short	V			

TABLE OF U8901/U8902		
Vendor	P/N	LCFC P/N
TI	SN74LVC1G66DCK	SA00005BE0J
NXP	74LVC1G66GW	SA00007KS00
ONsemi	MC74VHC1G66DFT2G	SA00008JQ00



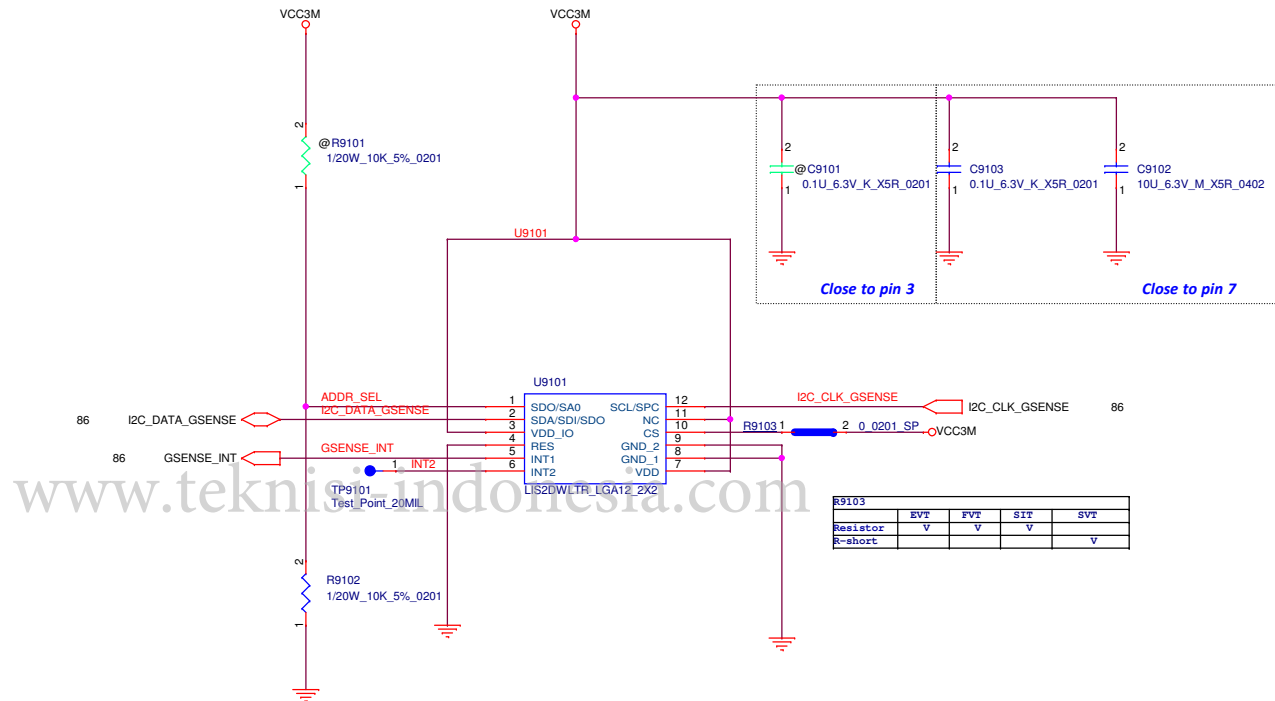
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Issued Date	2018/01/12	Deciphered Date	2018/01/12	FAN CONNECTOR	
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				Date:	Friday, December 28, 2018
				Sheet	90 of 125
				Rev	0.1




HDD Support	VCC3M
SSD Only	VCC3B

P/N	ADDR_SEL	Address
LIS2DWLTR	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX022-1020	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

TABLE of G-Sensor (U9101)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00




R9103				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

Security Classification		LC Future Center Secret Data		Title				
Issued Date	2018/01/12	Deciphered Date	2018/01/12	APS G-SENSOR				
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				Date:	Friday, December 28, 2018
				Sheet	92 of 125



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Rev 0.1

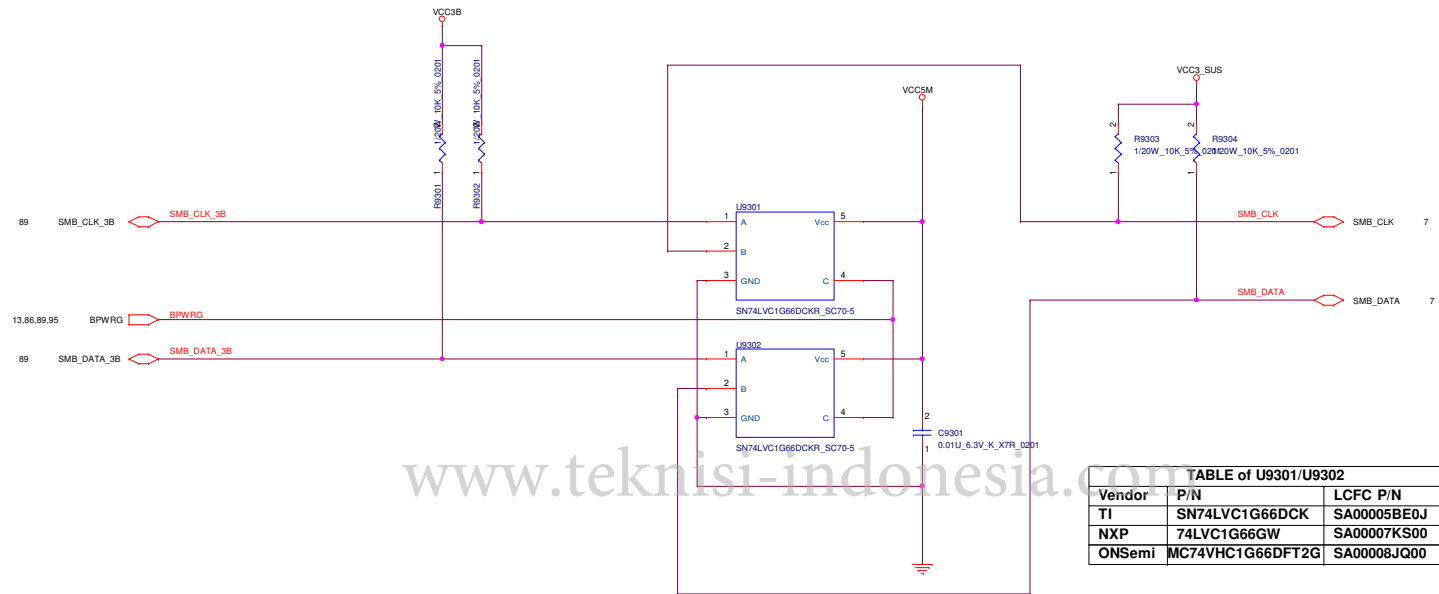
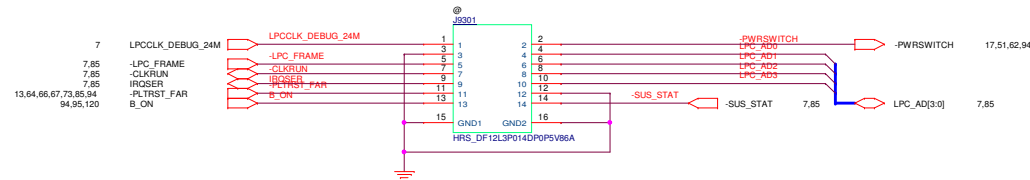


TABLE of U9301/U9302		
Vendor	P/N	LCFC P/N
TI	SN74LVC1G66DCK	SA00005BE0J
NXP	74LVC1G66GW	SA00007KS00
ONsemi	MC74VHC1G66DFT2G	SA00008JQ00

TABLE		
REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R220	ASM	NO_ASM

LOGIC



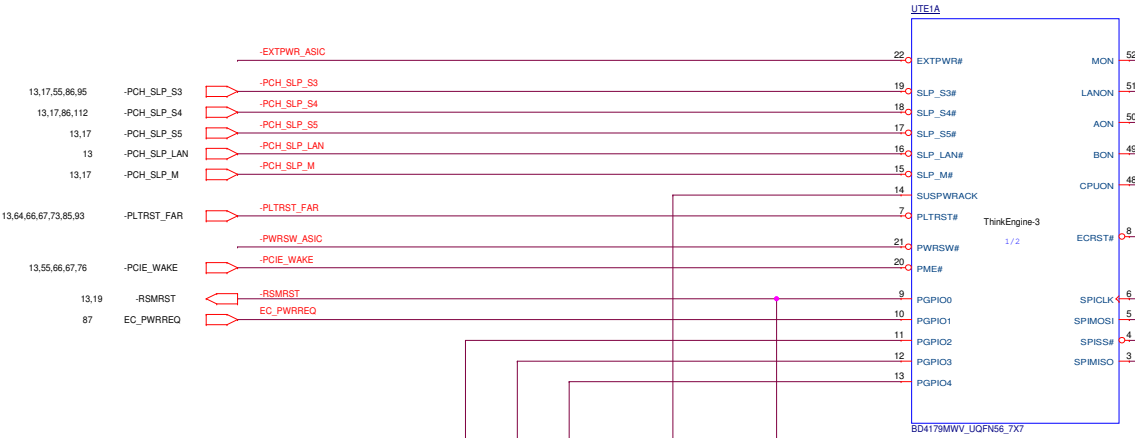
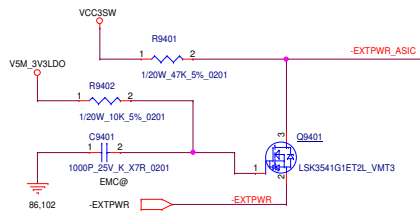
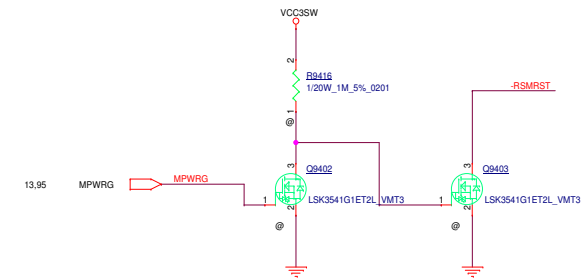
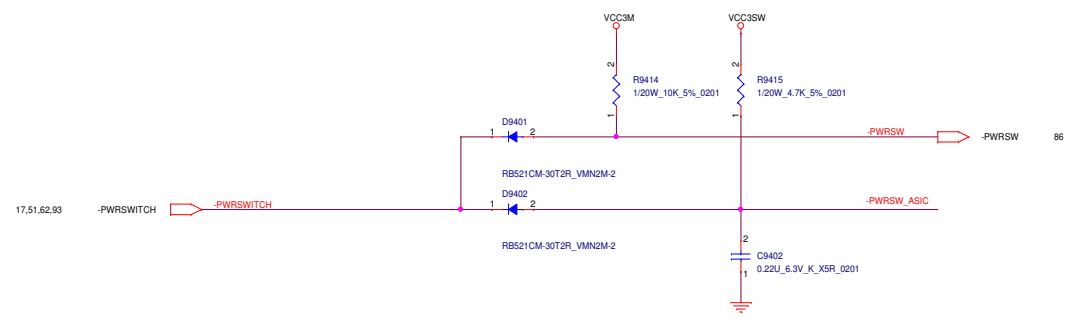
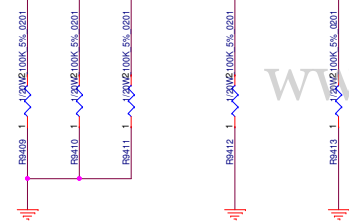
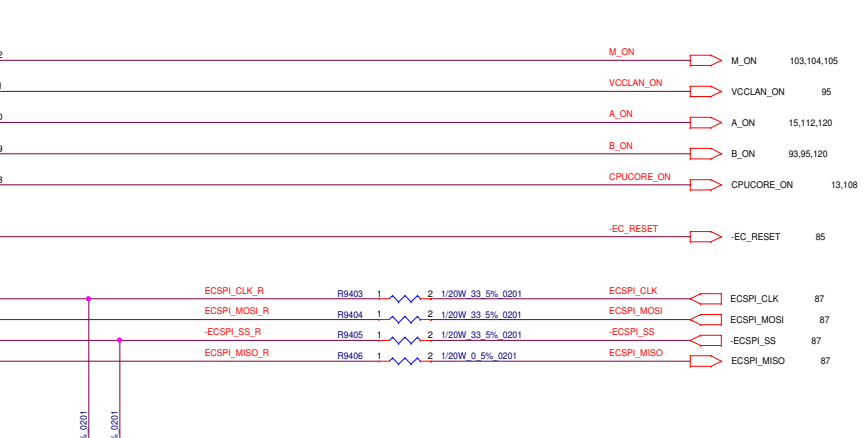


TABLE of UTE1		
Vendor	P/N	LCFC P/N
ROHM	BD4179MWV	SA000090J00
TOSHIBA	TC62D518FTG	SA00008E500




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				Date:	Friday, December 28, 2018	1 Sheet	94 of 125

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Date:				Friday, December 28, 2018	Sheet 95 of 125

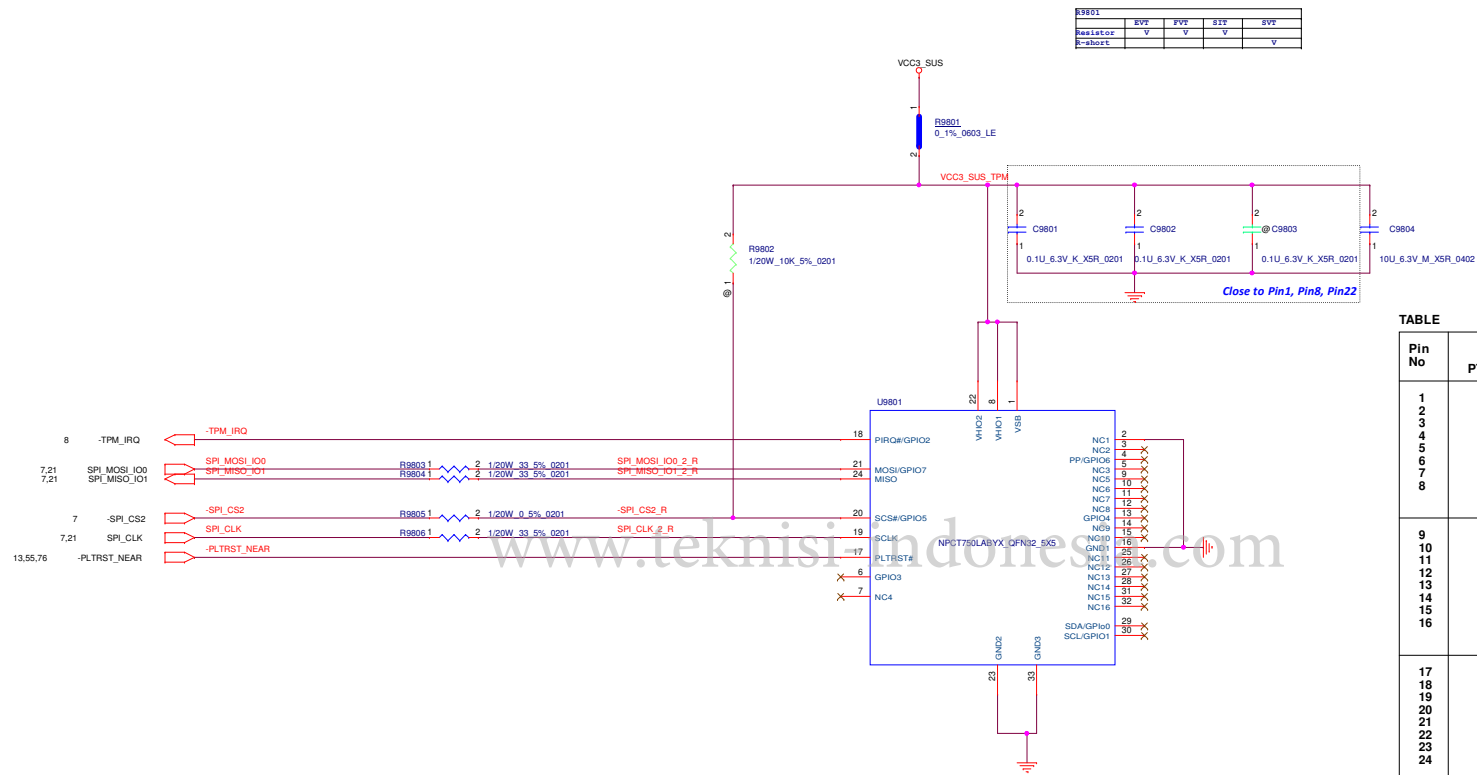


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				Custom			0.1
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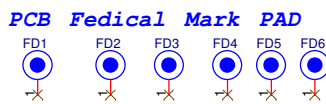
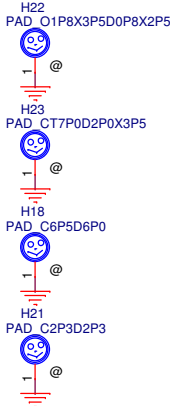
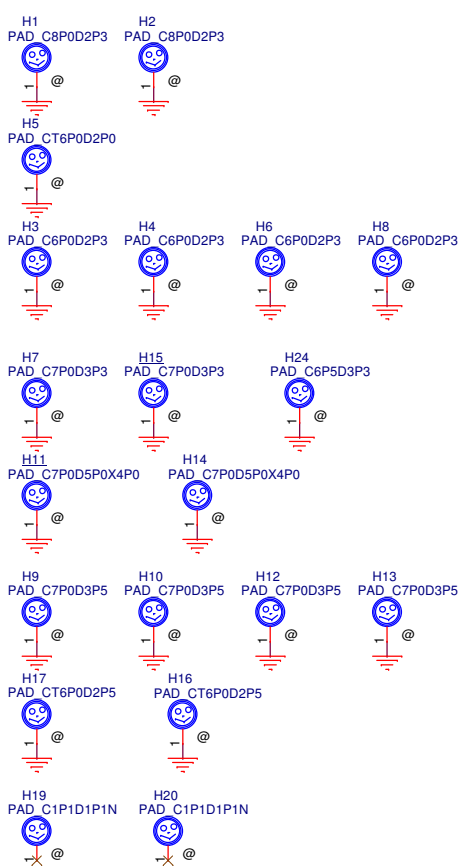
R9801	SWP	PVP	STV	SVV
Resistor	V	V	V	V
Short				V

TABLE

Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HTPH2E32AHC0
1	VDD	VS	NC
2	GND	NC	GND
3	NC	GPIO/PP	NC
4	GPIO	NC	PP
5	GPIO	GPIO3	NC
6	GPIO	NC	GPIO
7	VDD	VHIO	NC
8			
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	VDD	MOSI/GPIO7	MOSI
22	VHIO	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC

TABLE of TPM (U9801)		
Vendor	P/N	LCFC P/N
ST Micro	ST33HTPH2E32AHC0	SA000089E20
Nuvoton	NPCT750LABYX	SA00008KS10

R9805	SWP	PVP	STV	SVV
Resistor	V	V	V	V
Short				V



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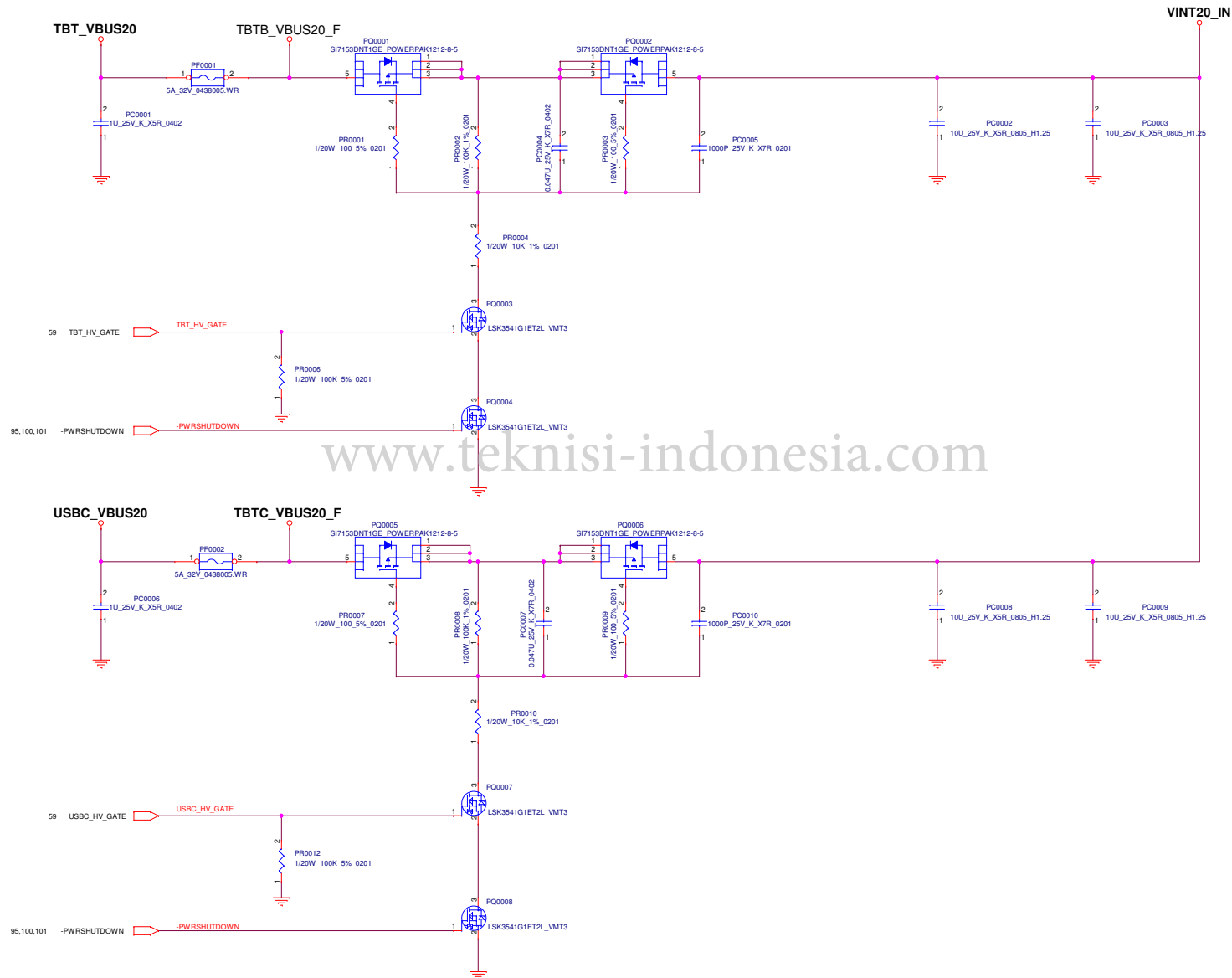
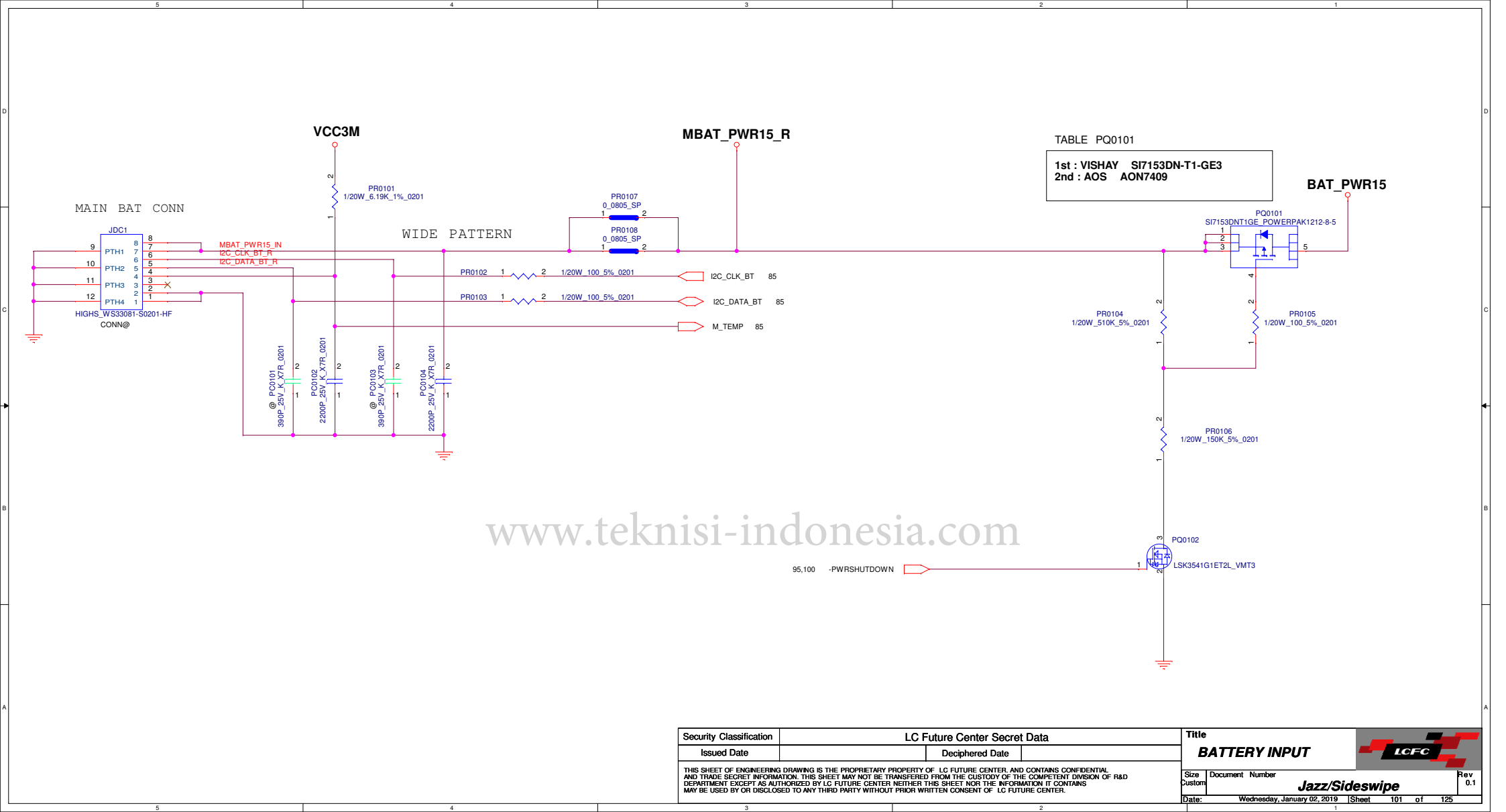
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Date:		Friday, December 28, 2018		Sheet 99 of 125			

TABLE PQ0001,PQ0002,PQ0005,PQ0006

1st : VISHAY SI7153DN-T1-GE3
2nd : AOS AON7409





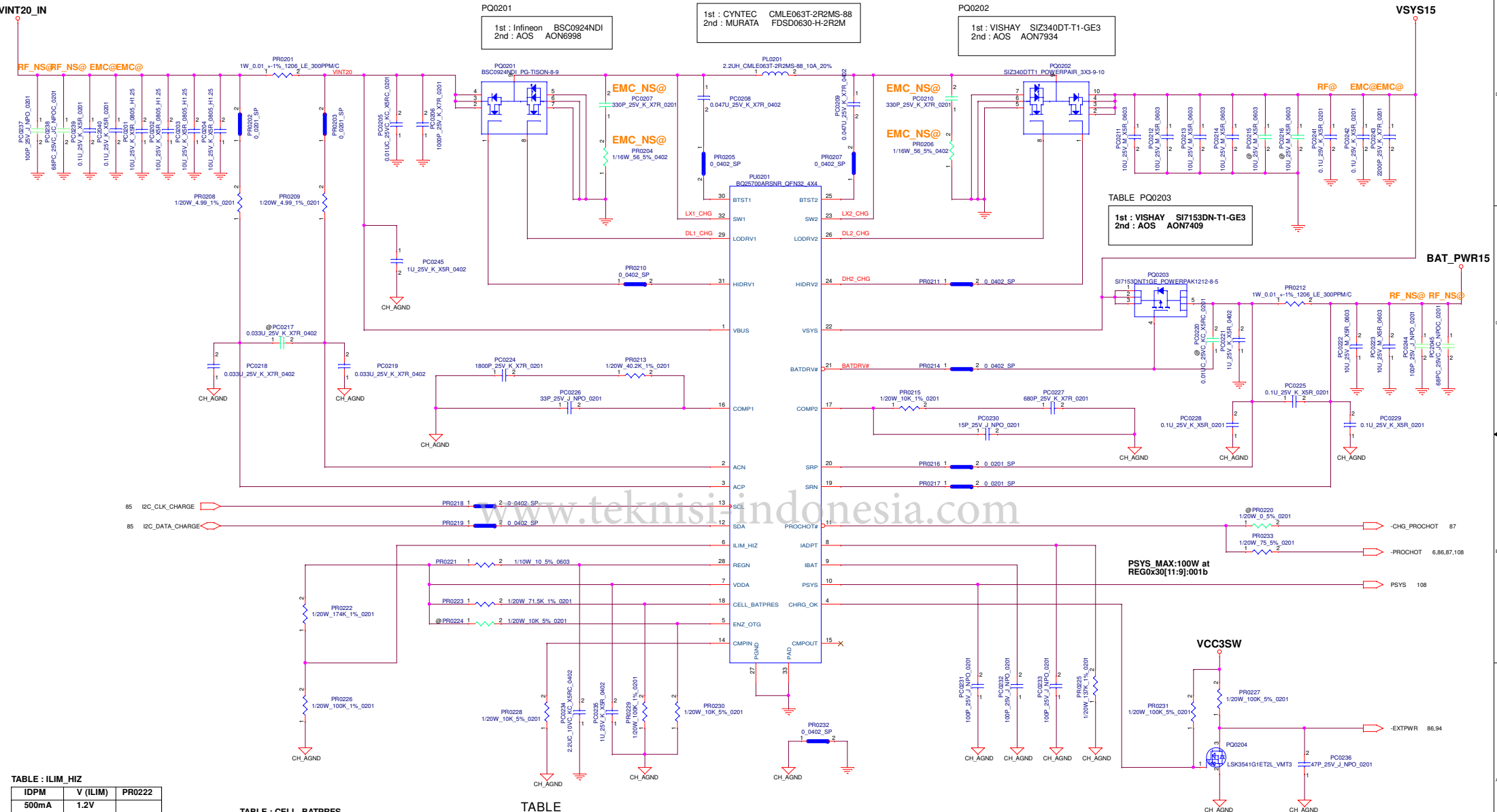


TABLE : ILIM_HIZ

IDPM	V (ILIM)	PR0222
500mA	1.2V	
1.0A	1.4V	
1.5A	1.6V	
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

TABLE : CELL_BATPRES

# of CELL	V (CELL_PRES)	PR0223
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

TABLE

Inductor	R(IADP)	fsw@POR
1.0uH	93kohm	800kHz
2.2uH	137kohm	800kHz
3.3uH	169kohm	800kHz

Security Classification

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Title

BATTERY CHARGER(BQ25700A)

Size

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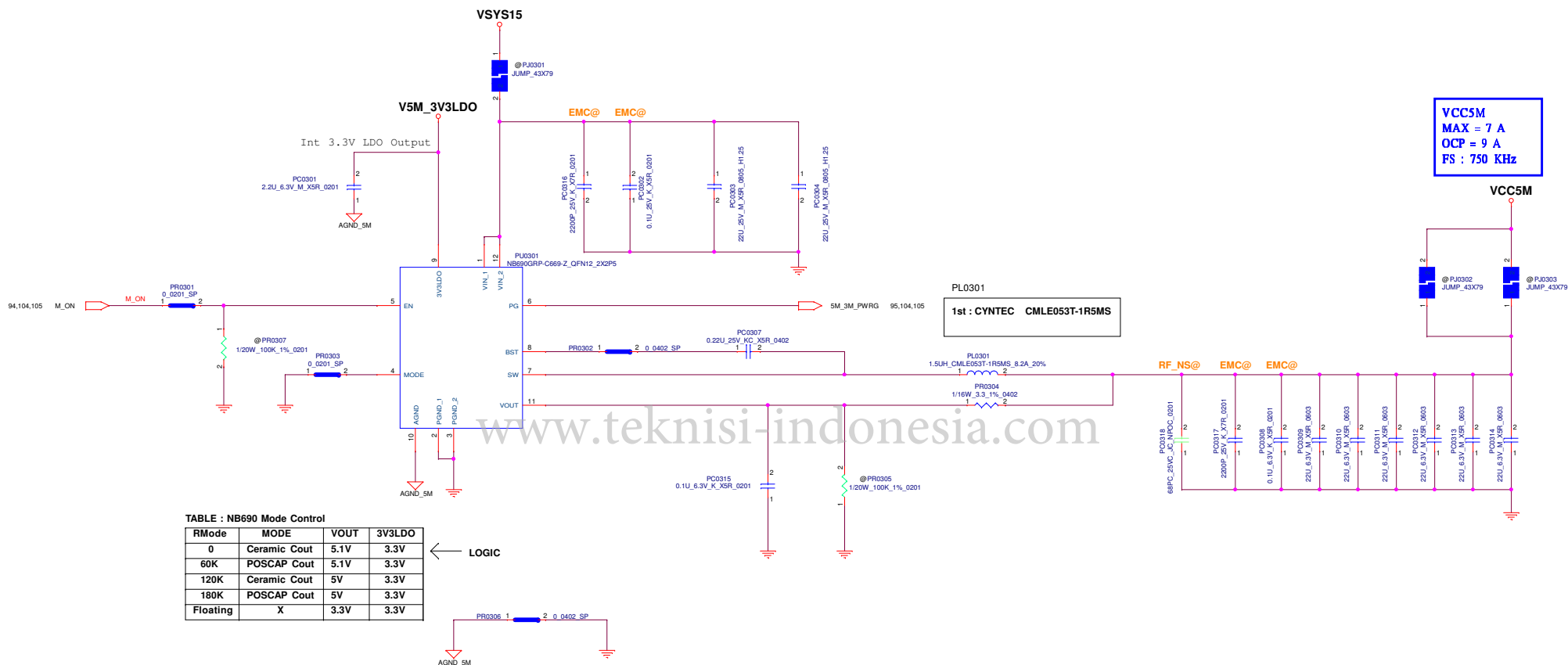
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VSYS15

@ PJ0501
JUMP_43X79

RF_NS@ EMC@ EMC@

PC0517 68PF_25V_K_NPOC_0201
PC0518 220PF_25V_K_X7R_0201
PC0522 0.1U_25V_K_X5R_0201
PC0520 22U_25V_M_X5R_0605_H1_25
PC0524 22U_25V_M_X5R_0605_H1_25

94,103,104 M_ON

PC0515 1U_6.3V_M_X5R_0201

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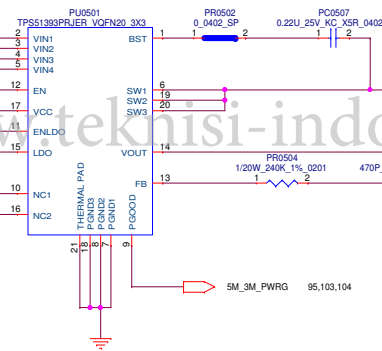


Table PL0501
1st : CYNTEC CMLE053T-1R5MS

VCC3M
MAX = 8 A
OCP = 9.6 A


VCC3M

@ PJ0502 JUMP_43X79 @ PJ0503 JUMP_43X79

RF_NS@ EMC@ EMC@

PC0519 68PF_25V_K_NPOC_0201
PC0529 220PF_25V_K_X7R_0201
PC0528 0.1U_25V_K_X5R_0201
PC0509 22U_6.3V_M_X5R_0603
PC0510 22U_6.3V_M_X5R_0603
PC0511 22U_6.3V_M_X5R_0603
PC0512 22U_6.3V_M_X5R_0603
PC0513 22U_6.3V_M_X5R_0603
PC0514 22U_6.3V_M_X5R_0603

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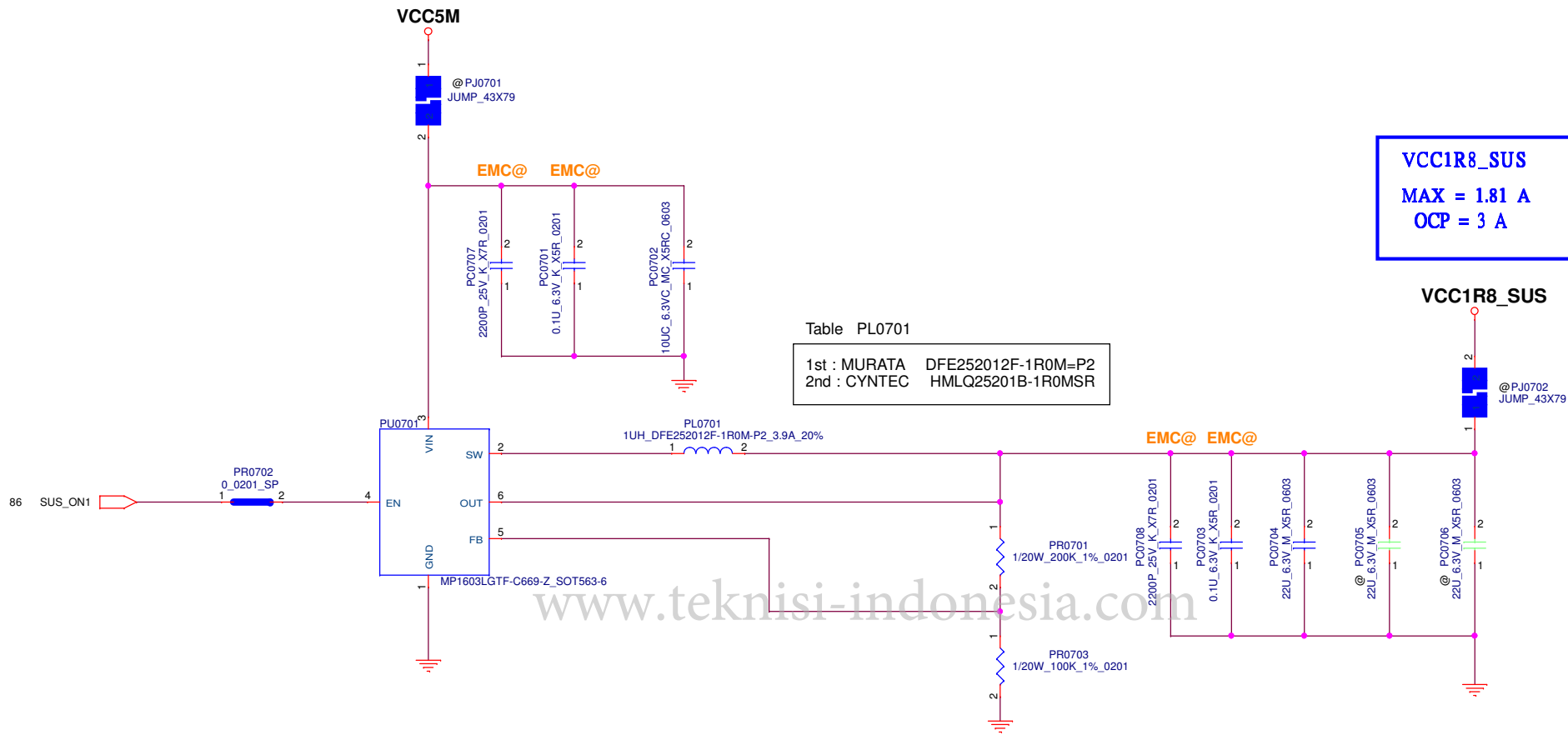
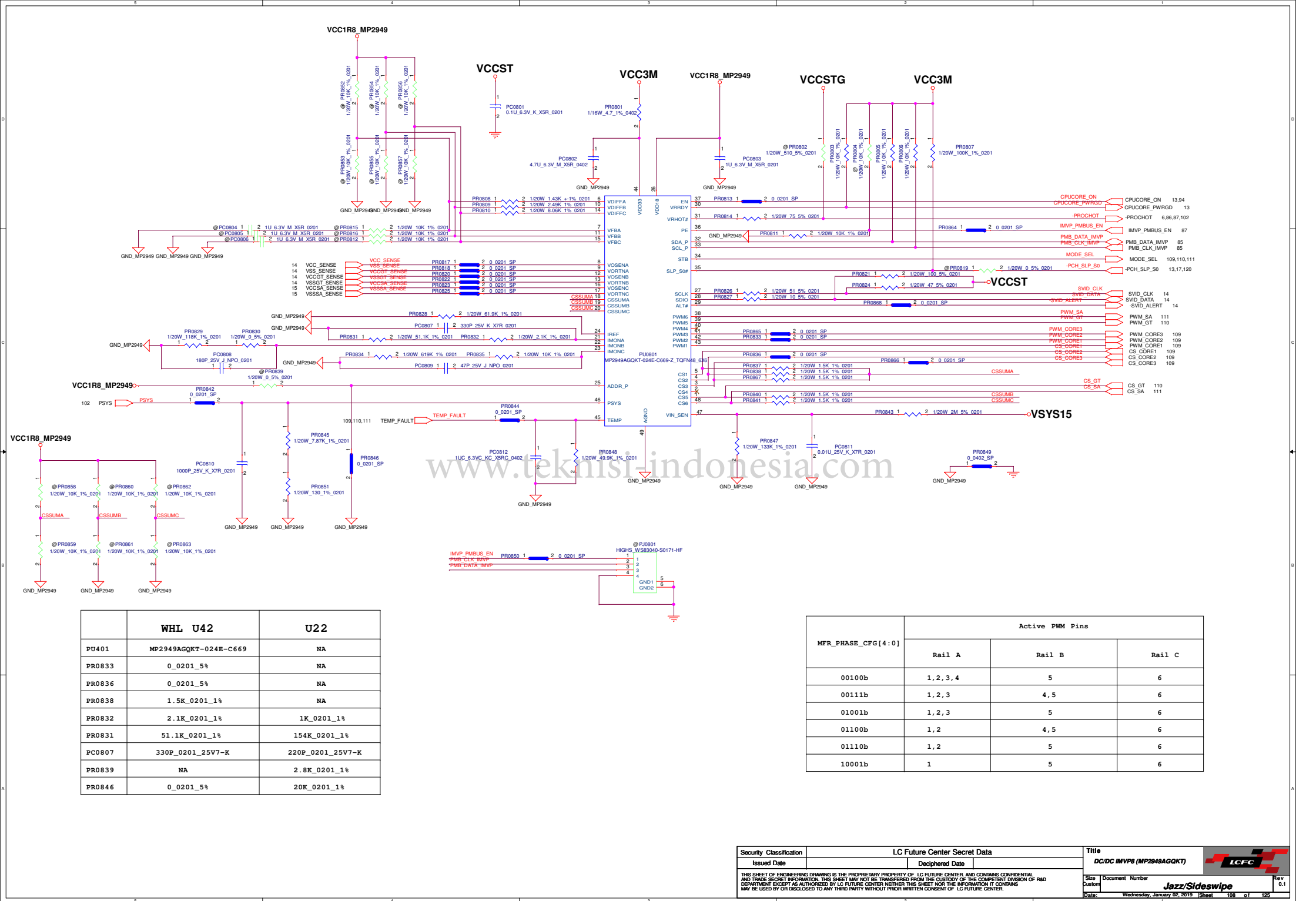
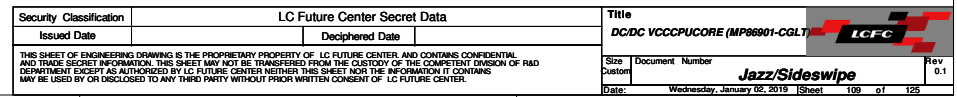


Table PL0701

1st : MURATA	DFE252012F-1R0M-P2
2nd : CYNTEC	HMLQ25201B-1R0MSR

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			Jazz/Sideswipe	
			Date:	Wednesday, January 02, 2019
			Sheet	107 of 125
			Rev	0.1





VCCGFXCORE_I

Panasonic	ETPE330MA9L
NEC TOKIN	TEPSGB20E337M9
KEMET	T520B337M2R5ATE009



Table

SYNC (MODE_SEL)	
High	Normal Operation
H.Z.	Standby Mode
Low	Diode Emulation Mode

VCCGFXCORE_I

TDC= 18A
IccMax= 31

TABLE PL1002

1st : CYNTEC CMLE062E-R15MS0R907-88

VCCGFXCORE_I

EMC@ EMC@

VSYS15

EMC@

PL1101
MPZ1608S300AT_2P-D

EMC@ EMC@ RF_NS@

For WHL VCCSA
8pcs 22uF+7pcs 10uF+7pcs 1uF

VCC3M

Table


SYNC (MODE_SEL)	
High	Normal Operation
H.Z.	Standby Mode
Low	Diode Emulation Mode

TABLE PL1102

CYNTEC CMLB051H-R33MS-88
NEC-Tokin MPLCH0520LR33

VCCSA
TDC= 4A
IccMax= 6A

VCCSA

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B	Jazz/Sideswipe				0.1
Date:	Wednesday, January 02, 2019		Sheet	111	of 125

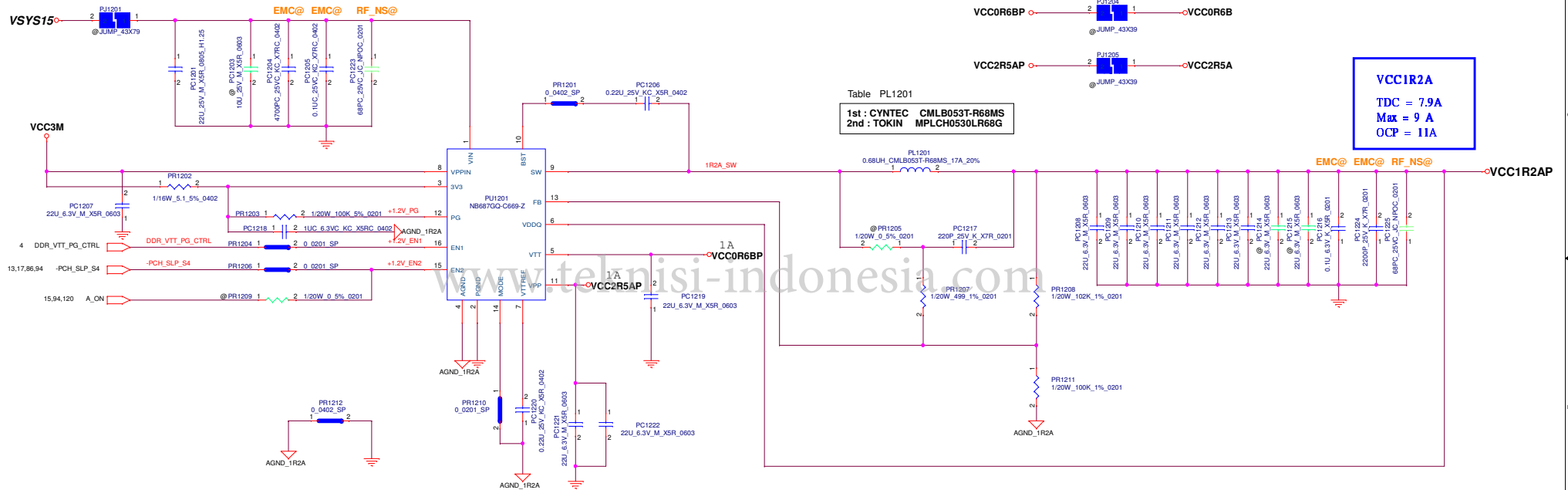



TABLE NB687GQ:EN1/EN2

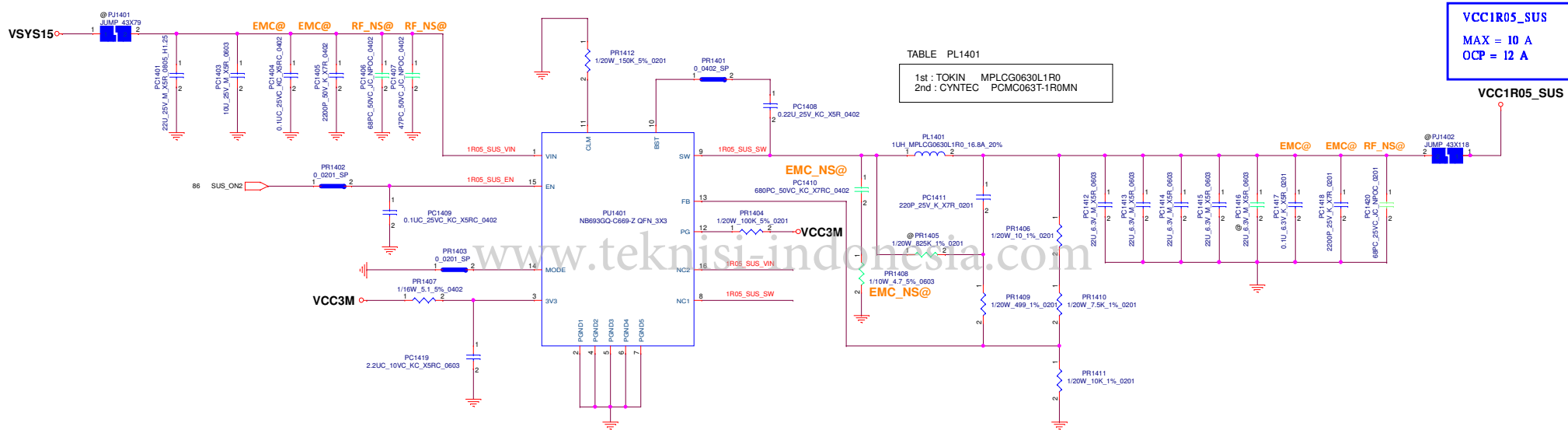
State	EN1	EN2	VDDQ	VTTREF	VTT	VPP
S0	High	High	ON	ON	ON	ON
S3	Low	High	ON	ON	OFF (High-Z)	ON
S4/S5	Low	Low	OFF	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF	OFF

TABLE NB687GQ:MODE

State	USM	Fs	Resistor to GND
M1	NO	700KHz	0
M2	YES	700KHz	90K
M3	NO	500KHz	150K
M4	YES	500KHz	>230K or Float

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				Jazz/Sideswipe	
Date:				Wednesday, January 02, 2019	Sheet 116 of 125



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B						0.1
Date:		Wednesday, January 02, 2019		Sheet 117 of 125		


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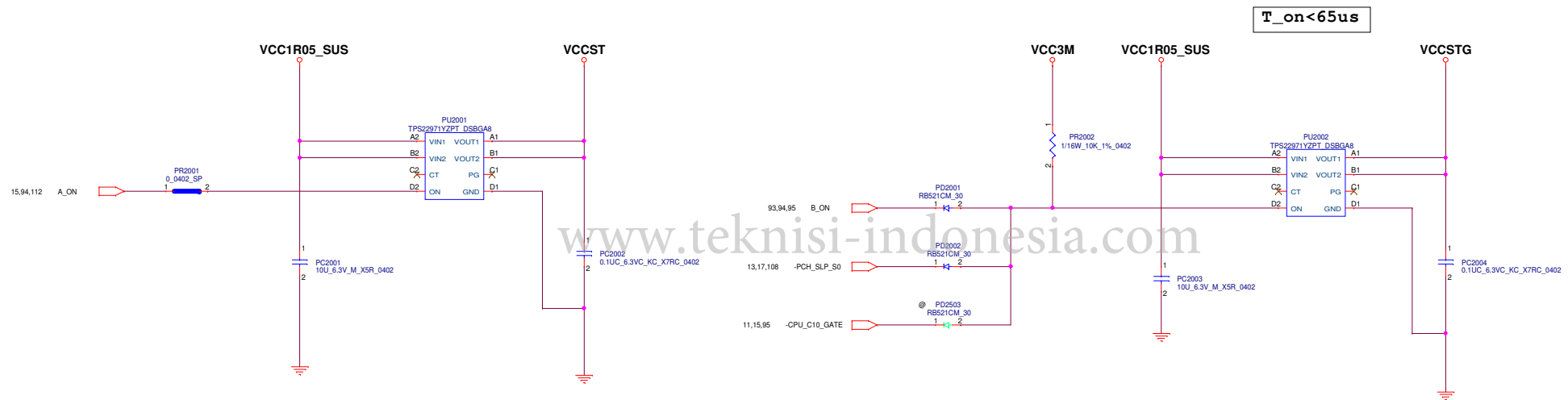
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B						0.1
Date:		Wednesday, January 02, 2019		Sheet 119 of 125		



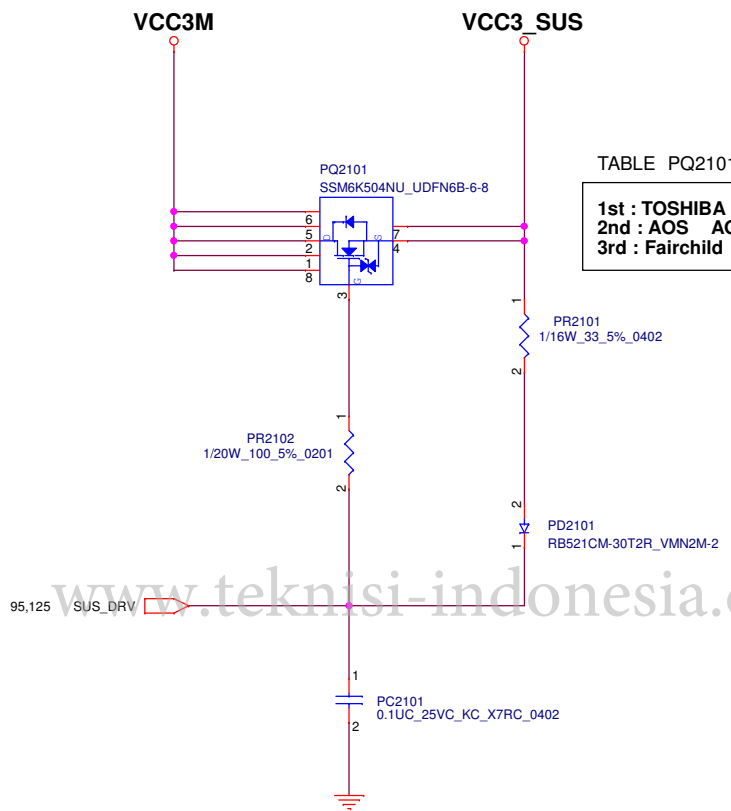



TABLE PQ2101


1st :	TOSHIBA	SSM6K504NU
2nd :	AOS	AON2420
3rd :	Fairchild	FDMA8878

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Date:				Wednesday, January 02, 2019 12:22 of 125		

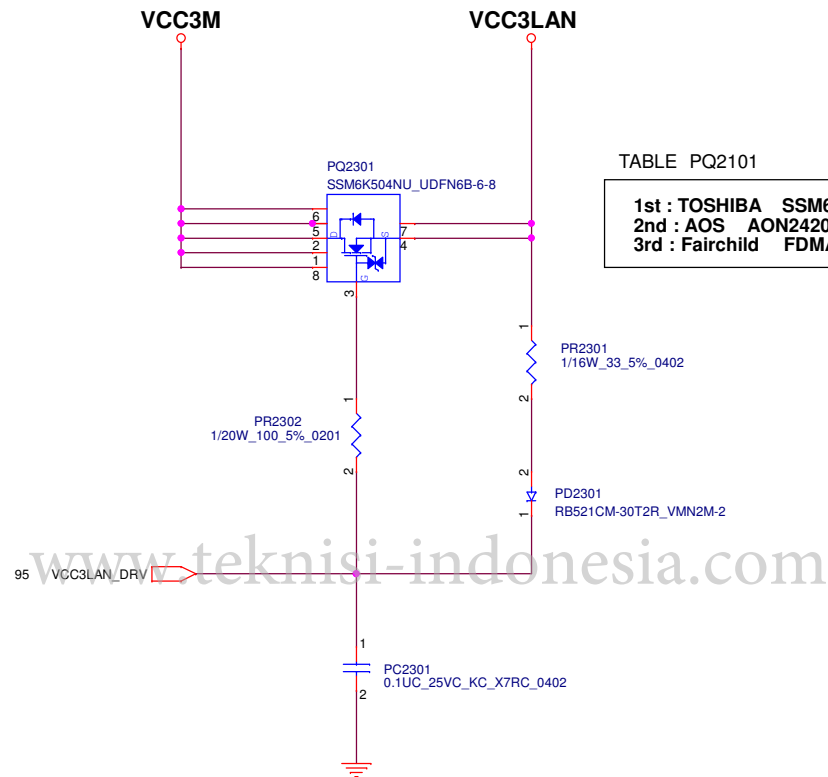

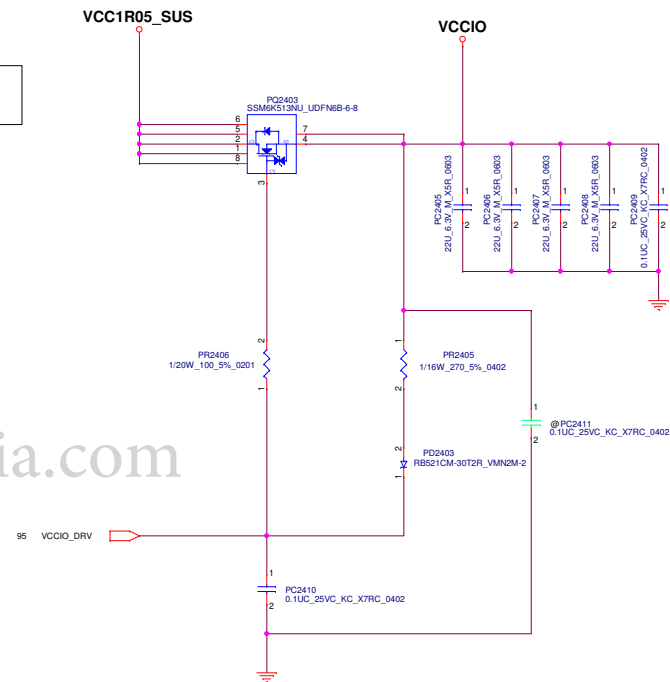
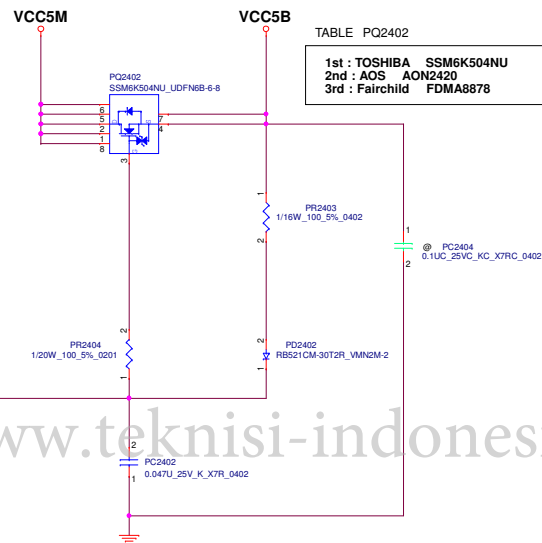
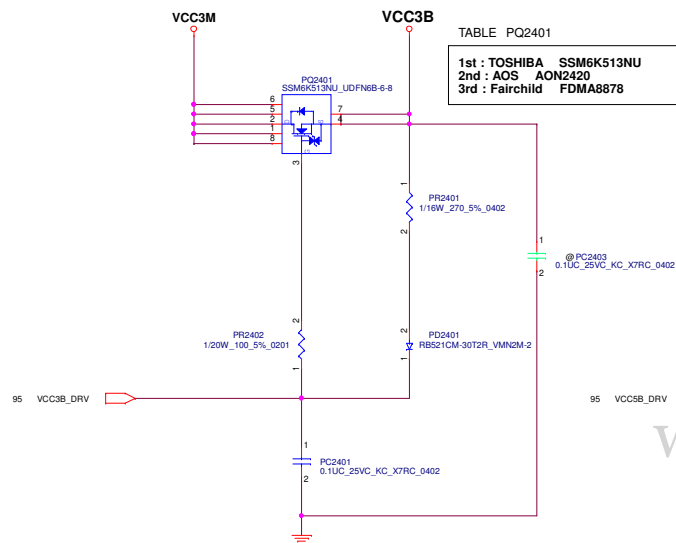
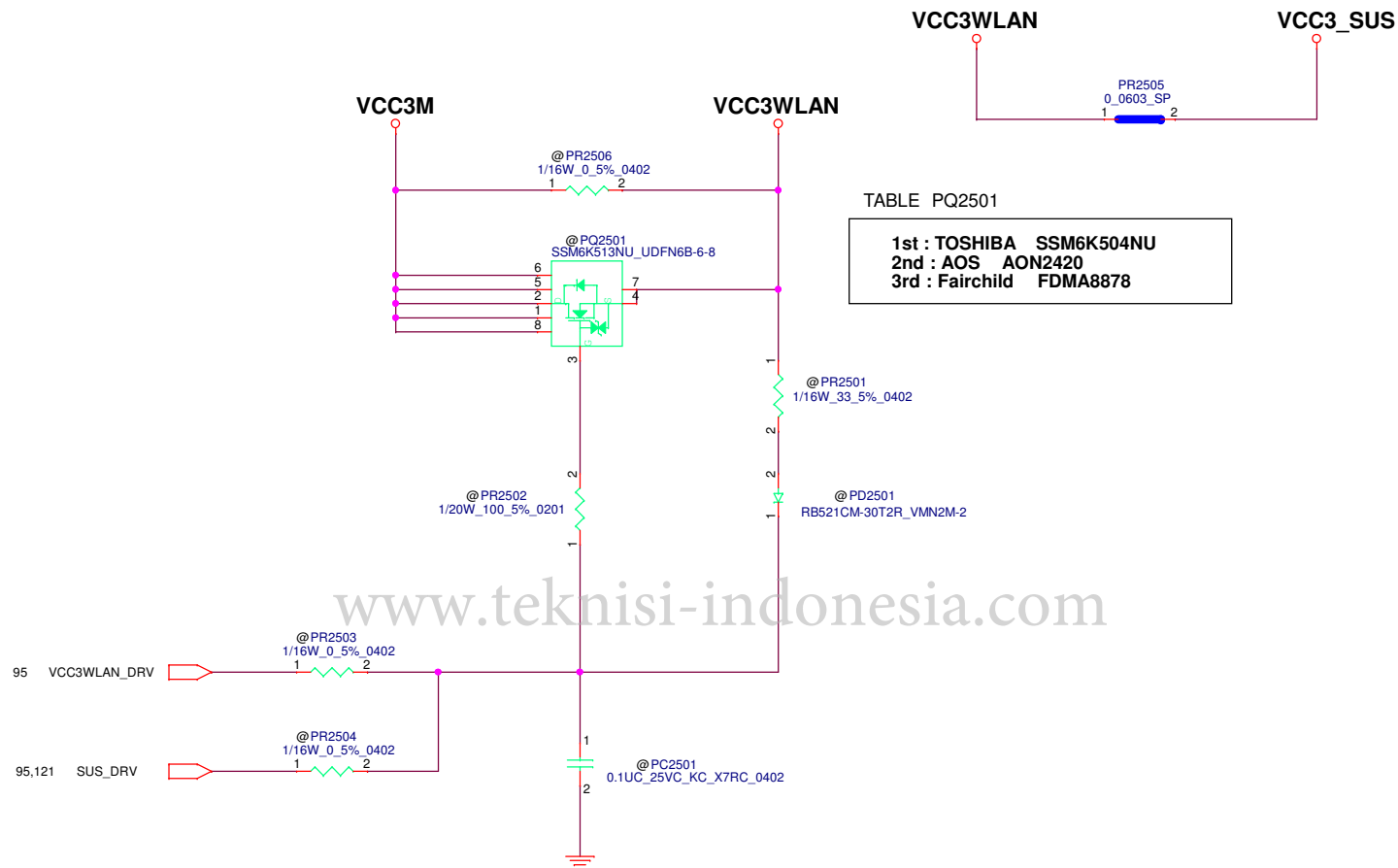



TABLE PQ2101

1st : TOSHIBA SSM6K504NU
2nd : AOS AON2420
3rd : Fairchild FDMA8878

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Date:	Wednesday, January 02, 2019		Sheet	123	of 125	





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